

TSRI 微縮光阻處理系統

TEL CLEAN TRACK ACT™ 8Z

標準製程總覽

Standard Process Overview

設備定位 Equipment Scope
光阻塗佈、烘烤、冷卻、曝光後烘烤、顯影及相關晶圓/破片處理。
Photoresist coating, baking, cooling, post-exposure bake, development, and related wafer/chip-substrate processing.

設備 / Equipment	TEL CLEAN TRACK ACT™ 8Z Coater / Developer
系統配置 / Configuration	2C2D Coater / Developer Track
適用基板 / Supported Substrates	6 吋與 8 吋晶圓，支援一般矽晶圓及透明材質晶圓；另支援 25 mm × 25 mm 破片之自動塗佈與顯影。 6-inch and 8-inch wafers, including standard silicon and transparent-material wafers; automated coating and development are also supported for 25 mm × 25 mm chip substrates.
文件用途 / Purpose	對外設備與製程能力介紹 / External equipment and process capability overview

本文件提供設備標準製程架構之概覽，實際製程條件依樣品、材料與服務需求確認。

This document provides a general overview of the standard process framework. Actual process conditions are confirmed according to sample, material, and service requirements.

1. 設備與製程概述

Equipment and Process Overview

TEL CLEAN TRACK ACT™ 8Z 為自動化光阻塗佈與顯影系統，可整合晶圓進料、表面前處理、光阻塗佈、烘烤、冷卻、曝光後烘烤、顯影、清洗及乾燥等製程步驟，並支援 25 mm × 25 mm 破片之自動塗佈與顯影製程。

The TEL CLEAN TRACK ACT™ 8Z is an automated photoresist coating and developing system that integrates wafer loading, surface preparation, resist coating, baking, cooling, post-exposure bake, development, rinsing, and drying operations, and also supports automated coating and development of 25 mm × 25 mm chip substrates.

6 / 8 吋晶圓與 25 mm × 25 mm 破片

6-inch / 8-inch wafers & 25 mm × 25 mm chip substrates

支援標準晶圓製程及破片自動塗佈/顯影。

Supports standard wafer processing and automated chip-substrate coating/development.

光阻塗佈

Photoresist Coating

可依光阻材料與目標膜厚建立製程條件。

Process conditions can be configured for resist type and target film thickness.

透明材質晶圓

Transparent-material wafers

可依適用條件進行自動化搬送與製程。

Automated handling and processing are available under qualified conditions.

顯影處理

Development

整合顯影、清洗與旋乾流程。

Integrates development, rinsing, and spin drying.

2. 標準製程流程

Standard Process Flow

塗佈流程 / Coating Flow

晶圓進料 Wafer Load	表面前處理 Surface Preparation	冷卻 Cooling	光阻塗佈 Resist Coating	邊緣/背面清潔 Edge & Backside Clean	軟烘烤 Soft Bake	冷卻/出料 Cool / Unload
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曝光後顯影流程 / Post-Exposure Development Flow

曝光完成 After Exposure	曝光後烘烤 Post-Exposure Bake	冷卻 Cooling	顯影 Development	清洗 Rinse	旋乾 Spin Dry	完成/出料 Finish / Unload
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生手快速理解：塗佈與顯影標準流程

Beginner Quick Guide: Standard Coating and Development Flows

以下流程以「每一步在做什麼」為主，讓第一次接觸微影製程的使用者快速建立概念。實際參數會依基板、光阻材料與服務需求確認。

The following guide focuses on what happens at each step so that first-time users can quickly understand the lithography workflow. Actual parameters are confirmed according to substrate, resist material, and service requirements.

A. 塗佈標準流程 / Standard Coating Flow

步驟 / Step	製程 / Process	生手理解 / Beginner Explanation	完成後狀態 / Result
1	基板確認與進料 Substrate Check & Load	確認 6 吋、8 吋晶圓或 25 mm × 25 mm 破片之尺寸、材質與表面狀態，再導入設備。 Confirm the size, material, and surface condition of the 6-inch wafer, 8-inch wafer, or 25 mm × 25 mm chip substrate before loading.	樣品正確進入自動製程 Sample correctly enters the automated flow
2	表面前處理 Surface Preparation	降低基板表面水氣並改善光阻附著性。可把它理解成「先把表面準備好，讓光阻黏得穩」。 Reduces surface moisture and improves resist adhesion — preparing the surface so the resist can adhere properly.	表面適合後續塗佈 Surface ready for coating
3	光阻供液與旋塗 Resist Dispense & Spin Coating	將光阻滴在基板上，再高速旋轉，使光阻展開成均勻薄膜。 Photoresist is dispensed onto the substrate and spread into a uniform thin film by spinning.	形成均勻光阻膜 Uniform resist film formed
4	邊緣/背面清潔 Edge / Backside Cleaning	移除邊緣或背面不需要的光阻殘留，降低後續搬送與製程污染風險。 Removes unwanted resist from the edge or backside to reduce contamination during later handling and processing.	邊緣與背面保持潔淨 Edge and backside kept clean
5	軟烘烤與冷卻 Soft Bake & Cooling	以受控加熱降低光阻中的溶劑，再冷卻至穩定狀態。 Controlled heating reduces solvent in the resist, followed by cooling to stabilize the coated substrate.	完成塗佈，可送往曝光 Coating complete; ready for exposure

塗佈完成後 → 進行曝光 → 再回到顯影流程

After coating → Exposure → Return for development

B. 顯影標準流程 / Standard Development Flow

步驟 / Step	製程 / Process	生手理解 / Beginner Explanation	完成後狀態 / Result
1	曝光後樣品進料 Post-Exposure Load	將已完成曝光的晶圓或破片導入顯影流程，並確認使用正確的製程條件。 Load the exposed wafer or chip substrate and confirm the appropriate process conditions.	曝光後樣品進入顯影流程 Exposed sample enters development flow

步驟 / Step	製程 / Process	生手理解 / Beginner Explanation	完成後狀態 / Result
2	曝光後烘烤（依光阻需求） Post-Exposure Bake (if required)	部分光阻在曝光後需要加熱，使曝光反應進一步完成，再進行冷卻。 Some resist systems require controlled heating after exposure to complete the intended reaction, followed by cooling.	光阻反應狀態穩定 Resist condition stabilized
3	顯影 Development	加入顯影液，選擇性移除應被去除的光阻區域，使曝光圖形逐漸顯現。 Developer selectively removes the intended resist regions so that the patterned image becomes visible.	圖形形成 Pattern formed
4	清洗 Rinse	以適用清洗流程停止顯影並帶走殘留顯影液與反應物。 Rinsing stops the development process and removes residual developer and reaction products.	表面完成清洗 Surface rinsed clean
5	旋乾與完成 Spin Dry & Finish	旋轉乾燥樣品，確認製程完成後再取出。 The sample is spin-dried and unloaded only after the process is confirmed complete.	完成顯影，可進行後續檢查或製程 Development complete; ready for inspection or next process

生手記憶方式 / Beginner Memory Aid

塗佈：把光阻「均勻地放上去」；曝光：把圖形「轉移到光阻」；顯影：把該去除的光阻「洗掉並留下圖形」。

Coating puts down a uniform resist film; exposure transfers the image into the resist; development removes the intended resist regions and reveals the pattern.

3. 主要製程功能

Key Process Functions

製程功能 Process Function	主要目的 Purpose	關鍵控制概念 Key Control Concept
晶圓進料與搬送 <i>Wafer Loading & Handling</i>	將晶圓或 25 mm × 25 mm 破片安全導入自動化製程流程。 <i>Safe loading and automated transfer of wafers or 25 mm × 25 mm chip substrates.</i>	尺寸、材質、表面/背面狀態及適用搬送條件。 <i>Size, material, front/backside condition, and qualified handling conditions.</i>
表面前處理 <i>Surface Preparation</i>	降低表面水氣並改善光阻附著性。 <i>Reduces surface moisture and improves resist adhesion.</i>	溫度、時間與材料相容性。 <i>Temperature, time, and material compatibility.</i>
光阻塗佈 <i>Photoresist Coating</i>	以旋塗方式形成均勻光阻膜。 <i>Forms a uniform photoresist film by spin coating.</i>	光阻種類、供液、轉速、時間。 <i>Resist type, dispense, spin speed, and time.</i>
邊緣/背面清潔 <i>Edge / Backside Cleaning</i>	移除晶圓邊緣及背面不必要的光阻或殘留。 <i>Removes unwanted resist or residue from wafer edge and backside.</i>	清洗液、供液位置與清洗條件。 <i>Cleaning chemistry, dispense position, and cleaning conditions.</i>
軟烘烤 <i>Soft Bake</i>	降低光阻溶劑含量並穩定膜層。 <i>Reduces solvent content and stabilizes the resist film.</i>	溫度、時間與冷卻條件。 <i>Temperature, time, and cooling conditions.</i>
曝光後烘烤 <i>Post-Exposure Bake</i>	依光阻系統完成曝光後所需反應。 <i>Completes the required post-exposure reaction for the resist system.</i>	溫度與時間。 <i>Temperature and time.</i>
顯影 <i>Development</i>	形成曝光圖案並移除對應區域光阻。 <i>Develops the exposed pattern by selectively removing resist.</i>	顯影液、供液、反應時間。 <i>Developer, dispense, and development time.</i>
清洗與乾燥 <i>Rinse & Dry</i>	停止顯影反應、清除殘液並完成乾燥。 <i>Stops development, removes residual chemistry, and dries the wafer.</i>	清洗與旋乾條件。 <i>Rinse and spin-dry conditions.</i>

4. 適用基板、透明材質晶圓與 25 mm × 25 mm 破片

Supported Substrates, Transparent-material Wafers, and 25 mm × 25 mm Chip Substrates

本系統支援 6 吋與 8 吋晶圓，包含一般矽晶圓及經製程評估確認之透明材質晶圓；另支援 25 mm × 25 mm 破片之自動塗佈與顯影製程。透明材質晶圓及特殊尺寸基板於使用前，需依材料特性與搬送條件確認適用性。

The system supports 6-inch and 8-inch wafers, including standard silicon wafers and qualified transparent-material wafers. It also supports automated coating and development of 25 mm × 25 mm chip substrates. For transparent or special-size substrates, process suitability should be confirmed according to material and handling characteristics.

確認項目 Verification Item	對外說明 External Description
晶圓尺寸 <i>Wafer Size</i>	確認使用 6 吋或 8 吋適用流程。 <i>Confirm the qualified process flow for 6-inch or 8-inch wafers.</i>
晶圓材質 <i>Wafer Material</i>	確認一般矽晶圓或透明材質晶圓之適用性。 <i>Confirm suitability for standard silicon or transparent-material wafers.</i>
表面/背面狀態 <i>Surface / Backside</i>	晶圓需保持完整、潔淨，並符合自動搬送條件。 <i>Wafers should be intact, clean, and suitable for automated handling.</i>
感測與對位 <i>Sensing & Alignment</i>	透明材質晶圓需確認設備感測與對位條件。 <i>Transparent-material wafers require confirmation of sensing and alignment conditions.</i>
製程配方 <i>Process Recipe</i>	依基板、光阻與目標規格使用經確認之製程條件。 <i>Use qualified process conditions according to substrate, resist, and target specification.</i>
25 mm × 25 mm 破片 25 mm × 25 mm Chip Substrate	確認破片尺寸、表面狀態及適用之自動塗佈/顯影條件。 <i>Confirm chip-substrate dimensions, surface condition, and qualified automated coating/development conditions.</i>

5. 關鍵製程控制項目

Key Process Control Parameters

控制項目 Control	中文說明	English Description
溫度 <i>Temperature</i>	前處理、軟烘烤、曝光後烘烤與冷卻。	Surface preparation, soft bake, post-exposure bake, and cooling.
時間 <i>Time</i>	烘烤、冷卻、顯影、清洗等步驟。	Bake, cooling, development, and rinsing steps.
旋轉條件 <i>Spin Conditions</i>	影響光阻膜厚、均勻性與乾燥效果。	Influences resist thickness, uniformity, and drying performance.
液體供應 <i>Chemical Dispense</i>	影響光阻塗佈、邊緣清潔、顯影與清洗。	Affects resist coating, edge cleaning, development, and rinsing.
製程路徑 <i>Process Flow</i>	依晶圓或破片尺寸、材質及製程目的使用適用流程。	Qualified flow is selected according to wafer/chip-substrate size, material, and process purpose.
材料相容性 <i>Material Compatibility</i>	確認基板、光阻、顯影液及後續曝光方式的相容性。	Confirms compatibility among substrate, resist, developer, and downstream exposure method.

6. 標準操作重點

Standard Operating Highlights

製程前確認 <i>Pre-process Check</i>	確認晶圓或破片尺寸、材質、表面/背面狀況及適用製程。 Confirm wafer or chip-substrate size, material, front/backside condition, and applicable process flow.
配方確認 <i>Recipe Verification</i>	確認所選製程與樣品、光阻及目標規格一致。 Confirm that the selected process matches the sample, resist, and target specification.
製程監控 <i>Process Monitoring</i>	製程期間依設備狀態顯示確認自動化流程正常執行。 Monitor equipment status during processing to ensure the automated flow proceeds normally.
完成確認 <i>Completion Check</i>	設備顯示製程完成後再進行晶圓取出。 Unload wafers only after the system indicates process completion.
異常處理 <i>Abnormal Condition</i>	如出現異常訊息，依現場作業規範聯繫設備管理人員。 If an abnormal message appears, follow site procedures and contact the equipment support personnel.

7. 曝光整合與應用

Exposure Integration and Applications

ACT8Z 可作為微影製程中的光阻塗佈與顯影平台，支援 6 吋、8 吋晶圓及 25 mm × 25 mm 破片，並可與適用的光學曝光或電子束曝光設備搭配，形成完整的微影製程流程。

The ACT8Z serves as a coating and development platform for 6-inch and 8-inch wafers as well as 25 mm × 25 mm chip substrates, and can be integrated with qualified optical or electron-beam exposure systems to form a complete lithography process sequence.

應用類型 Application	設備角色 System Role	說明 Description
光學微影 Optical Lithography	塗佈與顯影 Coating & Development	支援光阻塗佈、烘烤及曝光後顯影流程。 Supports resist coating, bake, and post-exposure development.
電子束微影 Electron-beam Lithography	光阻前後處理 Resist Processing	可依適用電子束光阻建立塗佈、烘烤與顯影條件。 Coating, baking, and development conditions can be configured for qualified e-beam resists.
透明基板應用 Transparent Substrate Applications	自動化晶圓處理 Automated Wafer Processing	依透明基板特性確認搬送、感測、塗佈與顯影條件。 Handling, sensing, coating, and development conditions are qualified according to transparent-substrate characteristics.
25 mm × 25 mm 破片製程 25 mm × 25 mm Chip-Substrate Processing	自動塗佈與顯影 Automated Coating & Development	支援 25 mm × 25 mm 破片之光阻塗佈、烘烤及顯影相關流程。 Supports photoresist coating, baking, and development workflows for 25 mm × 25 mm chip substrates.

8. 製程服務與條件確認

Process Service and Condition Confirmation

製程條件確認原則 Process Condition Confirmation

實際製程參數會依基板材質、尺寸、光阻種類、目標膜厚、曝光方式及圖形需求進行確認。對於透明材質晶圓、25 mm × 25 mm 破片或其他特殊基板，建議於正式製程前先完成適用性確認。

Actual process parameters are confirmed according to substrate material, size, resist type, target film thickness, exposure method, and pattern requirements. For transparent-material wafers, 25 mm × 25 mm chip substrates, or other special substrates, process suitability should be verified before formal processing.