Waiver of Liability for Chip Dicing and Packaging

The applicant, for the purpose of prototype chip research or educational needs, commissions the Taiwan Semiconductor Research Institute, National Institutes of Applied Research for chip dicing/packaging (Application no.: Package-OOO). The applicant agrees to assume the risks of scratching or damage during die clamping/vacuum-picking or of in-transit damage and other relevant risks not attributable to the Taiwan Semiconductor Research Institute, National Institutes of Applied Research.

Applicant

Professor's signature:

Affiliation (department/institute and university):

Tel.:

Email:

Date of application: