Guidance Notes and Instructions on Application for the Full-price Chip Service of Taiwan Semiconductor Research Institute, National Applied Research Laboratories

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I. Application Eligibility

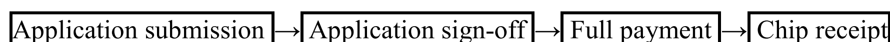
(I) Domestic academia: Applicants must be professors from domestic academic organizations (universities and colleges).

(II) Others: Please reach out to the contact before application.

II. Application Flow

(I) Domestic academia:

(II) Others:



III. Application Process

(I) Applicants must apply for process information with the TSRI and seek approval for its use before applying for chip manufacturing. If they have obtained the manufacturer's process information legally through other channels, please submit a "Declaration of Legal Use of Process Information for Chip Manufacturing."

(II) Applicants must log in to the TSRI website → Chip Implementation → Tape-out Application →Tape-out New Application to complete the following process prior to the chip manufacturing application deadline for each MPW schedule:

1. Fill out and submit a Full-price Chip Manufacturing Application Form
2. Send the files:
   - GDS file
   - Design information (only the chip layout or wire bonding diagram is needed)
   - DRC result (not required for P15, GaN25 and other WIN processes)
   - TRF document (only required for cell-based design projects)

IV. Process Code

(I) Announced processes:

Process code	Process name
TN16FFC	TSMC 16 nm CMOS LOGIC FinFET Compact (Shrink) LL ELK Cu 1P13M 0.8&1.8V
TN28HPM	TSMC 28 nm CMOS LOGIC High Performance Mobile Computing ELK Cu 1P10M 0.9&2.5V
AISOC	TSMC 28 nm CMOS LOGIC High Performance Mobile Computing ELK Cu 1P8M 0.9&1.8V
TN40G	TSMC 45 nm CMOS LOGIC General Purpose Superb (40G) ELK Cu 1P10M 0.9/2.5V
TN90GUTM	TSMC 90 nm CMOS Mixed Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0&3.3V (With UTM)
T18	TSMC 0.18 UM CMOS Mixed Signal RF General Purpose MiM FSG Al 1P6M 1.8&3.3V

SiGe18	TSMC 0.18 UM BICMOS Mixed Signal SiGe General Purpose Standard Process FSG Al 3P6M 1.8&3.3V
T18HVG2	TSMC 0.18UM CMOS HIGH VOLTAGE MIXED SIGNAL BASED GENERATION II BCD 1P6M SALICIDE AL_FSG 1.8/5/6/7/8/12/16/20/24/29/36/45/55/65/70V/VG1.8/5V AND 5/6/7/8/12/16/20/24/29/36/45/55/65/70V/VG5V
T25HVG2	TSMC 0.25UM CMOS HIGH VOLTAGE MIXED SIGNAL GENERAL PURPOSE IIA BASED BCD 1P5M SALICIDE NBL EPI AL USG 2.5/5/7/12/20/24/40/45/60V, VG2.5/5/12V
D35	TSMC 0.35 UM Mixed-Signal 2P4M Polycide 3.3/5V
(Applicable for D35) Multi-option-MEM	TSMC 0.35 UM CMOS Process and APM MEMS Process wi/wo Gold
T50UHV	TSMC 0.50 UM CMOS High Voltage Mixed Signal based LDMOS USG Al 2P3M 5/20/800V
U18	UMC 0.18 UM Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process
(Applicable for U18) U18MEMS	UMC 0.18 UM CMOS Process and MEMS Process
P15	WIN 0.15 UM PHEMT
GaN12	WIN 0.12um RF High Power GaN-on-SiC HEMT Technology
GIPD	General Purpose Integrated Passive Device (IPD) Process
IMEC-SiPh (iSiPP50G)	imec-ePIXfab SiPhotonics: iSiPP50G
IMEC-SiPh (Passives+)	imec-ePIXfab SiPhotonics: passives+

(II) For special requirements (like other processes), please reach out to the contact.

V. Tape-out Schedule

(I) Please refer to the Tape-out Schedule.

(II) For special requirements (like extra shuttle blocks), please reach out to the contact.

VI. Area Size

(I) Tape-out area size restrictions for the P15 and GaN25 processes:
All area sizes other than 1mm*1mm / 1mm*2mm / 1.5mm*1mm / 1.5mm*2mm / 2mm*1mm / 2mm*2mm / 2.5mm*1mm / 2.5mm*2mm / 3mm*1mm / 3mm*2mm / 3mm*3mm / 3mm*4mm are not accepted.

(II) Tape-out area size restrictions for the IMEC-SiPh (iSiPP50G) process: Smaller than 2.5mm*2.5 mm, 2.5mm*2.5 mm, 2.5mm*5.15 mm.

(III) Tape-out area size restrictions for the IMEC-SiPh (Passives+) process: Smaller than 5.15mm*2.5 mm, 5.15mm*2.5 mm, 5.15mm*5.15 mm.

VII. Notes

(I) Chip manufacturing applicants must carefully read the "Terms and Conditions for Full-price Chip Manufacturing." [Paragraphs 2, 3, and 4 of Article 7 and Paragraph 2 of Article 14 do not apply to the IMEC-SiPh process.]

(II) To makes changes to the application information submitted, chip manufacturing applicants must file a change application and update data/files within five weekdays after the application deadline. If a change application is filed after the deadline, the original application is used for chip manufacturing/packaging and the processing of payments.

(III) After an advanced chip is changed to a Full-price chip by filing an application for special requirements, it may not be changed back to an advanced chip.

(IV) Due to a limited number of blocks per MPW schedule for foundry shuttle processes, please make a booking three months before the respective application deadlines according to the schedule if applicants plan to manufacture large-area chips with shuttle blocks; otherwise, the TSRI cannot ensure that the foundries have sufficient blocks for tape-out.

(V) Chip manufacturing applicants must complete DRC verification and confirm the results and use the layer definitions defined by the TSRI for the layout. [Please refer to IMEC PDK process information for the use of IMEC-SiPh process layers.] For any technical problems with regard to layout or filling out a STI/MT form (only applicable to applications for large-area chip manufacturing using shuttle blocks), please reach out to the engineers in charge before application.

(VI) To increase the chip manufacturing success rate and take into account the fact that the sensitivity of circuit characteristics to dummy pattern filling varies, applicants must carefully deal with matters related to dummy pattern filling. For applications using cell-based design kits, applicants can choose whether the TSRI will perform dummy pattern filling after GDS file replacement. For all other types of circuits, applicants must perform dummy pattern filling by themselves. If a full-custom layout and a layout using a cell-based design kit exist simultaneously, please fill the dummy pattern in the full-custom layout region and use a layer to mark the full-custom layout region as a region to which the TSRI will not add a dummy pattern. For all unmarked regions (including the layout region using a cell-based design kit), applicants can choose whether the TSRI will fill the dummy pattern after GDS file replacement. (Please reach out to engineers in charge before application.) For dummy pattern filling by the TSRI, we can only do our best to make sure that the GDS file meets design principles. However, the TSRI does not guarantee that the dummy pattern will not cause any effects on the circuit. The TSRI is not responsible for remaking or any cost compensation (reimbursement) in the event of failed chip manufacturing under the application which is confirmed by the foundry to be caused by not filling the dummy pattern. [Please follow instructions on the IMEC PDK for IMEC-SiPh process dummy patterns.]

(VII) To use Full-price services with special requirements (e.g., packaging, dicing, flip-chip assembly), applicants must sign a Risk Assumption Consent Form. Please reach out to the contact

VIII. Application Billing Information

(I) Applicants are required to carefully read all contents before signing off the “Full-price Chip Manufacturing Quotation” (Full-price Chip Manufacturing Fee Sign-off Form), including terms and conditions for Full-price chip manufacturing. Applicants are deemed to have accepted all contents and confirmed this application form upon sign-off.

(II) Applicants should make relevant payments as soon as possible after signing off the “Full-price Chip Manufacturing Quotation” (Full-price Chip Manufacturing Fee Sign-off Form). Overdue payment: The TSRI will stop providing relevant services if payment is still not made after reminders, unless there are force majeure circumstances.

(III) Academic, research and industry applications are distinguished by their invoice headers. The headers of invoices issued by the TSRI for domestic academic applications should be the names of domestic academic organizations.

(IV) In principle, one single invoice is issued for one chip manufacturing/design application. If sponsored by multiple programs, please use an expense apportionment table for reimbursement with your organization, if possible.

(V) In principle, for domestic academic applications, the invoice will be sent together with chip shipment, with a 90-day payment term from the issuance of the invoice; for other applications, payment needs to be cleared before pickup/receipt of the chip.

(VI) To ask for an invoice first for reimbursement, if needed, please file a separate application for invoice pre-issuance.

(VII) Payment method:

1. T/T
   Bank name: Hsinchu Science Park Chu-tsuen Branch of Mega International Commercial Bank
   Account no.: 215-09-05345-0
   Account name: Taiwan Semiconductor Research Institute, National Applied Research Laboratories
2. Checks
   Made payable to: Taiwan Semiconductor Research Institute, National Applied Research Laboratories
   Please send checks by registered mail to: No. 26, Zhanye 1st Rd., Hsinchu Science Park, Hsinchu City 300-091

to Taiwan Semiconductor Research Institute - Payment Contact, Chip Implementation Service Division