This is a sample file (certain sections are omitted), and the default name of the calibre output file is cellname.lvs.summary.
Please send the original file in its original text format and keep the original content when uploading a file.

```
################################################
##                                            ##
##          C A L I B R E     S Y S T E M     ##
##                                            ##
##              L V S    R E P O R T          ##
##                                            ##
################################################
```

REPORT FILE NAME: circuit.lvs.report
LAYOUT NAME: circuit.calibre.db
SOURCE NAME: [redacted]
RULE FILE: [redacted]
RULE FILE TITLE: [redacted]
LVS MODE: Mask
RULE FILE NAME: [redacted]
CREATION TIME: Fri Oct 23 11:12:36 2009
CURRENT DIRECTORY: [redacted]
USER NAME: [redacted]
CALIBRE VERSION: v2009.2_36.21 Tue Jul 7 15:59:45 PDT 2009

****

OVERALL COMPARISON RESULTS

****

```
      #        ###################        _   _
     #         #                 #       *   *
  #    #       #      CORRECT    #           |
   # #          #                #        \___/
    #           ###################
```

NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	4	4	
Nets:	4	4	
Instances:	1	1	MN (4 pins)
	1	1	MP (4 pins)
Total Inst:	2	2	

****

LVS PARAMETERS

****

o LVS Setup:

```
// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY
// LVS PIN NAME PROPERTY
LVS POWER NAME                    "VCC" "VDD" "VDD3V" "DVDD" "V3IO" "V2IO"
LVS GROUND NAME                   "VSS" "GND" "VBB" "V0IO" "DGND"
LVS CELL SUPPLY                   NO
LVS RECOGNIZE GATES               ALL
LVS IGNORE PORTS                  NO
LVS CHECK PORT NAMES              NO
LVS IGNORE TRIVIAL NAMED PORTS    NO
LVS BUILTIN DEVICE PIN SWAP       YES
```

```
LVS ALL CAPACITOR PINS SWAPPABLE          NO
LVS DISCARD PINS BY DEVICE                NO
LVS SOFT SUBSTRATE PINS                   NO
LVS INJECT LOGIC                          YES
LVS EXPAND UNBALANCED CELLS               YES
LVS EXPAND SEED PROMOTIONS                NO
LVS PRESERVE PARAMETERIZED CELLS          NO
LVS GLOBALS ARE PORTS                     YES
LVS REVERSE WL                            NO
LVS SPICE PREFER PINS                     NO
LVS SPICE SLASH IS SPACE                  YES
LVS SPICE ALLOW FLOATING PINS             YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS          NO
LVS SPICE CONDITIONAL LDD                 NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS      NO
LVS SPICE IMPLIED MOS AREA                NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS                NO
LVS SPICE REDEFINE PARAM                  NO
LVS SPICE REPLICATE DEVICES               NO
LVS SPICE SCALE X PARAMETERS              NO
LVS SPICE STRICT WL                       NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                       NO
LVS EXACT SUBTYPES                        NO
LAYOUT CASE                               NO
SOURCE CASE                               NO
LVS COMPARE CASE                          NO
LVS DOWNCASE DEVICE                       NO
LVS REPORT MAXIMUM                        50
LVS PROPERTY RESOLUTION MAXIMUM           32
// LVS SIGNATURE MAXIMUM
LVS FILTER UNUSED OPTION                  AB RC RE RG
// LVS REPORT OPTION
LVS REPORT UNITS                          YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
```

// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS NO
LVS REDUCE PARALLEL MOS YES
LVS REDUCE SEMI SERIES MOS NO
LVS REDUCE SPLIT GATES NO
LVS REDUCE PARALLEL BIPOLAR YES
LVS REDUCE SERIES CAPACITORS YES
LVS REDUCE PARALLEL CAPACITORS YES
LVS REDUCE SERIES RESISTORS YES
LVS REDUCE PARALLEL RESISTORS YES
LVS REDUCE PARALLEL DIODES YES
LVS REDUCTION PRIORITY PARALLEL

// Trace Property

TRACE PROPERT
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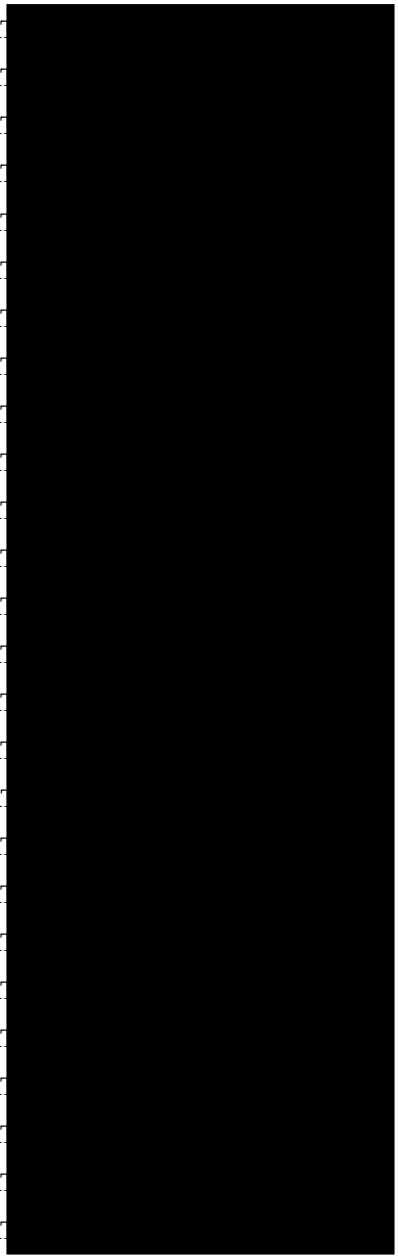

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INFORMATION AND WARNINGS

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Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
---	---	---	---	---

Ports:	4	4	0	0	
Nets:	4	4	0	0	
Instances:	1	1	0	0	MN(N_18)
	1	1	0	0	MP(P_18)
	-------	-------	---------	---------	
Total Inst:	2	2	0	0	

o Initial Correspondence Points:

Ports: vi vdd! gnd! vo

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SUMMARY

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Total CPU Time: 0 sec

Total Elapsed Time: 1 sec