[1] Name and telephone number of the designer

Do not list the names of the instructor or school.

Name of student: Chang Hsiao-Ming

Tel.: 0912345678, 03-5773693 # 999

[2] Project name

Project name in Chinese: 25GHz low-power CMOS differential oscillator

Project name in English**:** A 25GHz Current Reused Differential Oscillator

[3] Recent three tape-out records

Tape-out MPW Schedule and chip number	Project name	Measurement result:
T18-97C-001	5GHz low noise amplifier	function work
T18-100C-034	Low-frequency CMOS differential oscillator	partial work

[4] New Design or Description of Revised Version

Description: Select and provide pertinent explanations using the three categories below:
(1) The designer's new design; (2) a revision of an earlier design completed by the designer; and (3) the adoption of another designer's design for improvement.

- If the design falls under (1) the designer's new design, the existing design will not be revision. Please specify "This case is the designer's new design" in this item;

- If the design falls under (2) a revision of an earlier design completed by the designer or (3) the adoption of another designer's design for improvement, please specify "This case is a revision of an earlier design completed by the designer" or "This case is the adoption of another designer's design for improvement" in Item [4] New design or description of revised version. The need for a tape-out revision, the specifications of previous tape-out versions, and

measurement results should be clarified. In addition, the content of the current revision and the improved specifications should be explained (if the measurement results of the previous version are not normal, the reason chips fail to act normally should be analyzed in order to achieve better results during reviews).

"This case is a revision of an earlier design completed by the designer" The following are some related descriptions: This case was taped out in MPW ScheduleT18-100C. Following measurement, the obtained oscillation frequency is lower (around 20GHz), falling short of the specification requirements (24.5GHz). As a result, in order to meet the specifications, the design must be modified and then taped out.

Following an examination of the chip measurement results of the T18-100C MPW Schedule, it was determined that the lower oscillation frequency is the result of ( ). To reduce disparities between simulation and measurement, ( ) is improved, ( ) is modified, ( ) is added during simulation, and other relevant variables that may cause impacts are included in this design. Furthermore, the component sizes and overall layout are optimized to reduce power consumption, resulting in a smaller chip area. A comparison of T18-100 chips and the specifications of this design case is as shown in the table below:

Parameter	T18-100C chips	This work
Result	Measurement	Post-sim(tt)
Process	0.18um	0.18um
Power Supply (V)	2	2
Total Current (mA)	1.24	1.17
Power Dissipation (mW)	2.48	2.34
Oscillator Frequency (GHz)	20.7	24.15
Phase Noise (dBc/Hz@1MHz)	-108.2	-108.2
Output Power (dBm)	-8	-6.5
Chip size (mm^2)	0.55 x 0.8	0.477 x 0.742

[5] Current status of related research and

development

The rapid growth of the wireless communications market in recent years has boosted global research and development in related fields...

[6] Research Motivation

In the oscillator, the performance of local oscillation is determined; in terms of traditional CMOS oscillator circuit design…

[7] Introduction to architecture

Please provide textual or illustrative explanations of the architecture and circuit diagram of this design case. If there are reference diagrams and circuit diagrams, please place them [4] in related research development situations or [5] research motivation. When the design architecture is extensive, the design structures and circuits should be divided into multiple diagrams and each should be elaborated upon separately. When external components or circuits are required, the completed vector architecture should be elaborated.

As shown in Figure 1 (a), the drain current of the transistor is $(-Ix/SC_1)\ g_m$ ...

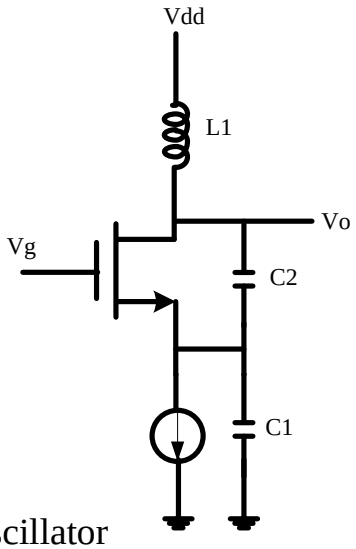
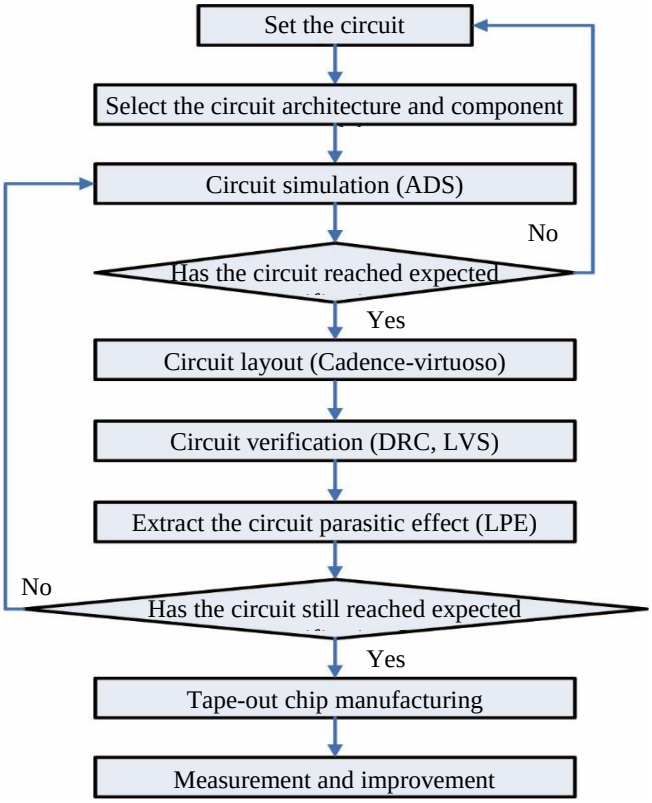


Figure 1 (a) NMOS Colpitts oscillator

[8] Design processes

Please provide textual or illustrative explanations of

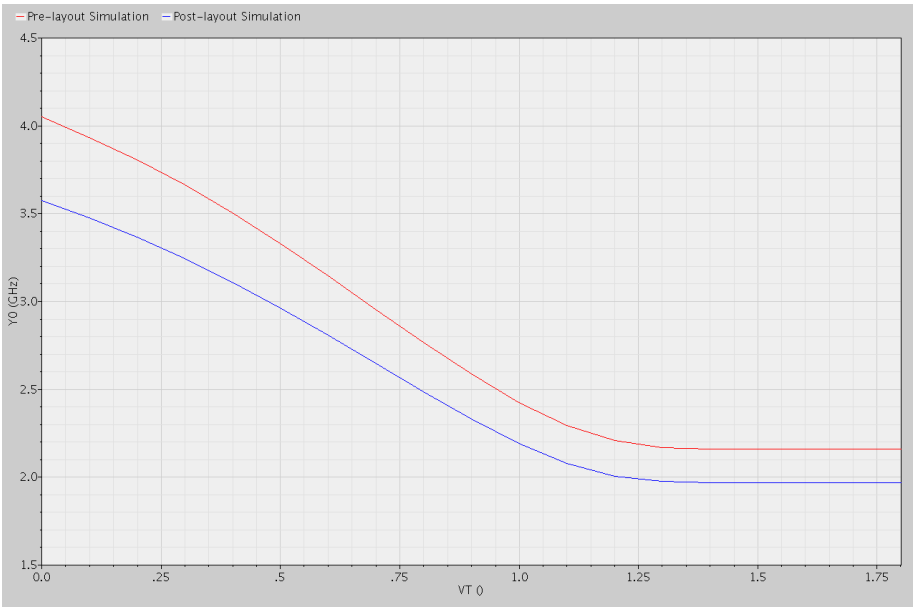
the design processes.
Example:



[9] Simulation results

Please list the results of the comparison between pre-layout simulation and post-layout simulation.

Example 1: (Curve overlap)


Pre-layout Simulation
Post-layout Simulation
4.5
4.0
3.5
3.0
2.5
2.0
1.5
Y0 (GHz)
0.0
.25
.5
.75
1.0
1.25
1.5
1.75
VT 0

Example 2: (Represented by two diagrams)

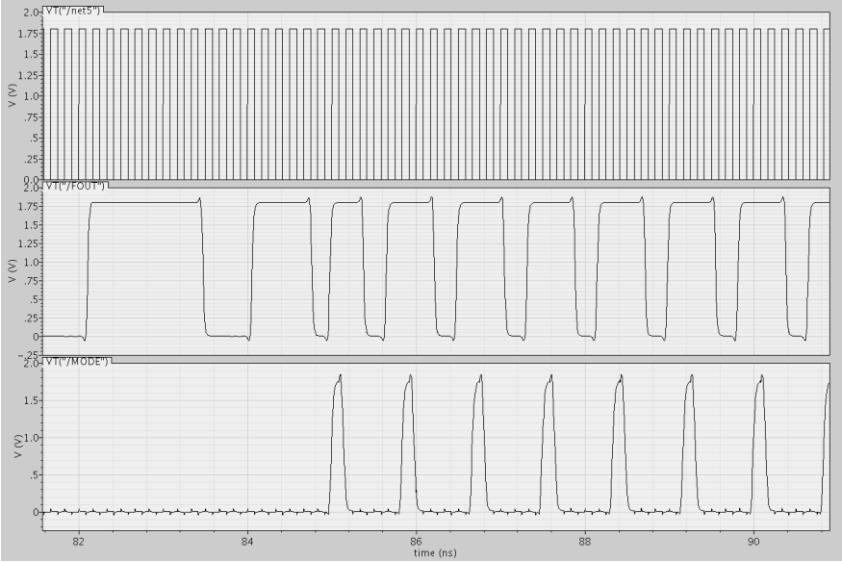


Fig.1 (a) Pre-layout Simulation

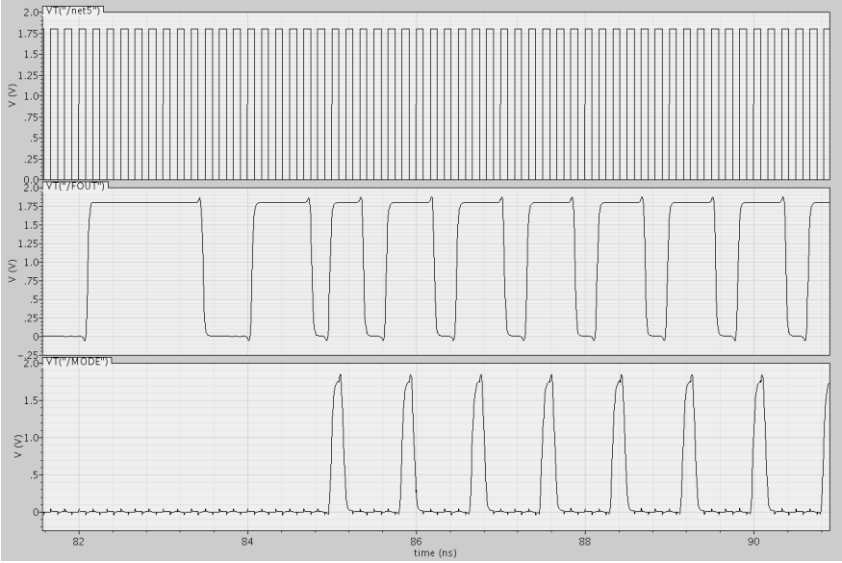


Fig.1 (b) Post-layout Simulation

Example 3: (shown in tables)

Corner Case simulation

RF Corner	FF	TT	SS
Oscillator Frequency (GHz)	24.15	24.15	24.15
Phase Noise (dBc/Hz@1MHz)	-108.8	-108.2	-108.7
Output Power (dBm)	-6.5(GHz)	-6.5(GHz)	-6.6(GHz)

[10] Measurement considerations

Please provide textual or illustrative explanations of the instrument setup and measurement procedures, among other things. Indicate the use of PCB, peripheral circuits, or components through text or illustrations. *It is unnecessary to specify the precise location of the measurement work.*

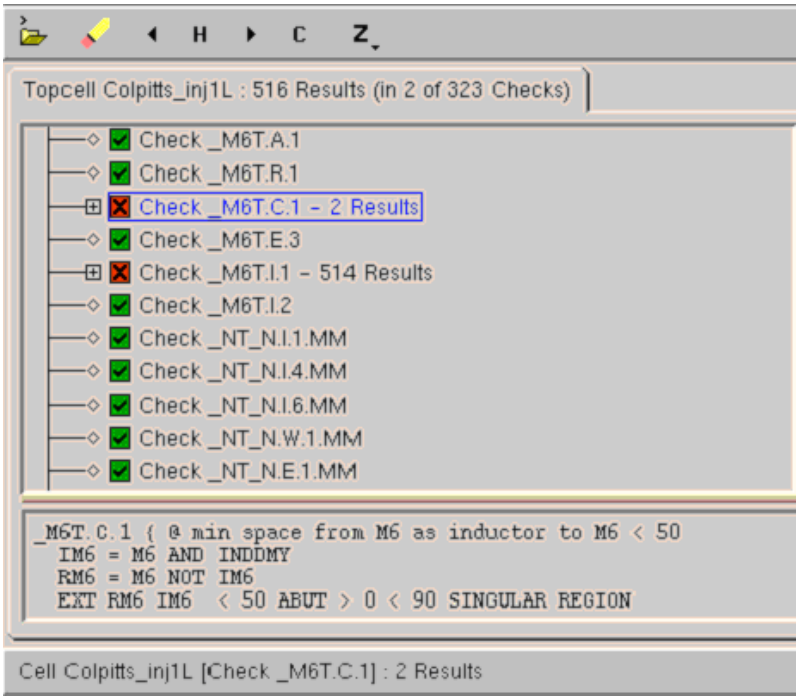
[11] Description of layout verification result errors

It is sufficient for results to *comprise a mere explanation of errors*. Simply indicate error-free verification results using DRC-OK and LVS-OK. Do not paste drc.results, drc.summary, or lvs.report contents here.

Example:

(A) DRC verification results:

Two errors have been found (as shown in the diagram below), which are allowable DRC errors.



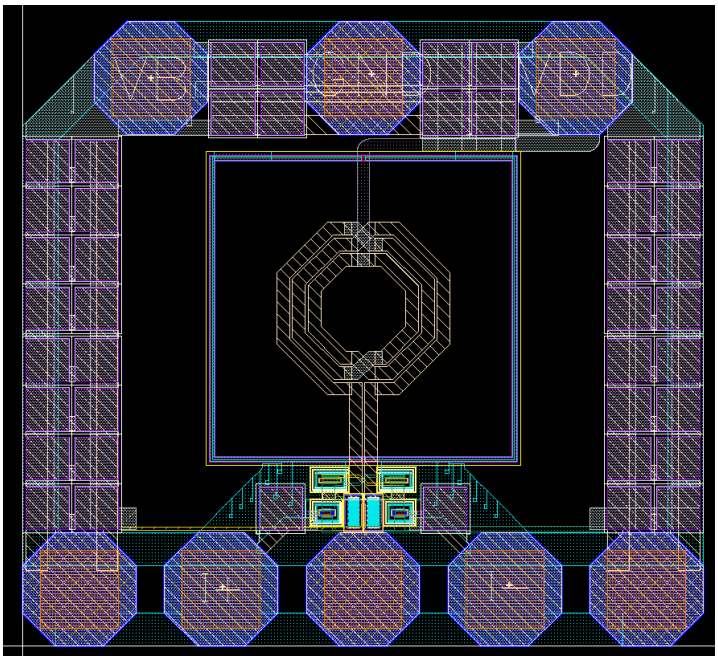
(B) LVS verification result files:

LVS-OK

[12] Layout plan

Please make sure the uploaded gds file chips and the photograph of this layout are identical.
Otherwise, the chip application will not be accepted.

Chip Size	:	0.477 x 0.742 mm^2
Transistor/Gate Count	:	4Transisotors
Power Dissipation	:	2.36mW
Max. Frequency	:	2.5GHz



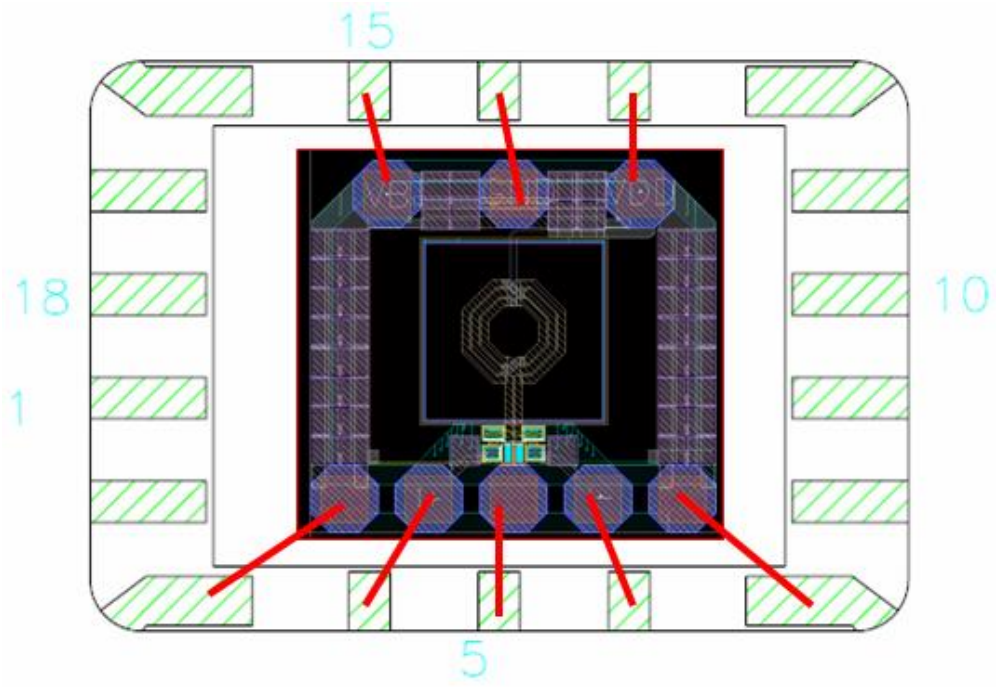
Layout diagram

[13] Wire bonding diagram

Applicants that choose not to package are required to specify (wiring is not required).

Example:

SB18



Wire bonding diagram

[14] Estimated Specifications Table

Please present provide tabulated results for the specification, pre-layout simulation, and post-layout simulation.

Example:

Parameter	**Spec.**	**Pre-sim(tt)**	**Post-sim(tt)**
Power Supply (V)	=2	2	
Total Current (mA)	<1.2	1.18	1.17
Power Dissipation (mW)	<2.4	2.36	2.34
Oscillator Frequency (GHz)	=24.5	24.53	24.15
Phase Noise (dBc/Hz@1MHz)	<-100	-106.3	-108.2
Output Power (dBm)	>-8	-7.6	-6.5
Chip size (mm^2)	<0.5x0.8	0.477 x 0.742	

[15] Performance Comparison Table

Please compare this design to the various specifications and FOM (Figure-of-Merit) (please also list the FOM formula) of related designs published in recent seminars and journal papers in a table. This

will allow reviewers to quickly gain insight into the aspects of this design that make it superior to others. Please specify if the design content consists of an entirely novel framework or system integration for which comparison references and designs are not accessible.

Parameter	This work	ISSCC20XX[5]	XXX Journal 20XX[6]
Result	Post-sim(tt)	Measurement	Measurement
Process	0.18um	0.18um	0.18um
Power Supply (V)	2	2	1.8
Total Current (mA)	1.17	1.3	1.5
Power Dissipation (mW)	2.34	2.6	2.7
Oscillator Frequency (GHz)	24.15	25	24
Phase Noise (dBc/Hz@1MHz)	-108.2	-99	-101
Output Power (dBm)	-6.5	-7.2	-7.0
Chip size (mm^2)	0.477 x 0.742	0.5 x 0.5	0.6 x 0.5
FOM	xxx	ooo	***

*FOM formula: FOM = ……

*The compared papers are listed in References

[16] References

[1] Ming-Da Tsai,“A 5-GHz Low Phase Noise Differential Colpitts CMOS VCO”, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS,VOL. 15, NO. 5, MAY 2005.