國家實驗研究院
NATIONAL INSTITUTES OF APPLIED RESEARCH

Example for TSRI Report

Note

- To ensure that review meetings are fairer, avoid mentioning applicant-related school departments, advisors, laboratory, identity, and other information in slides (including logos) and during the review report process.
- The tape-out MPW Schedule application number is used in handling during the review process.
- If negative review results are caused by a violation of regulations, one must accept responsibility!
- The slide format and page count are unrestricted, and the emphasis is on narratives. However, the content must contain the items referenced in the example below (these are items that reviewers frequently request).
- Please be sure to include page numbers on the slides for the convenience of committee review and questioning.

Review Meeting Report Example

國家實驗研究院
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鎖相迴路於脈波產生器之設計 (project name in Chinese)
Design on phase locked loops for clock generator
(project name in English)

Application No: SiG-094A-A0023

Date: 2005/04/16

Outline

- Introduction & Motivation
  (Including last three taped-out chip records)
- Architecture & Schematic
- Simulated Results
- Layout
- Specification Table
- Measured Considerations
  (Including instrument/measure Env. setup)
- References

Introduction & Motivation

- The last three taped-out chip records

Chip number (IC No.)	Project Name	Result/status
T18-93A-XX	**XXXXXX**	**Fail/ Work/ Partial work**
T18-93C-XX	**YYYYYY**	**going on****
none***		

** if you don't get the chip yet, fill in "going on"

*** if you don't have any chip implementation record, just to fill in "none"

- List motivations for this PLL.
- List contributions (feature) for this PLL.

Architecture & Schematic

- All schematic of PLL must be revealed clearly. (need to detail describe it during presentation.)
- Design principle of this new PLL can be explained briefly.

Simulated Results

- Simulated results/figures of this PLL must include all corner cases of process.
- Simulated results/figures of this PLL must be shown clearly.
- All parameter which need to measure must be description clearly.

Layout

- The layout of this PLL must be clearly revealed. (Its important for RF circuit)
- Clear node-notation in layout for this PLL is necessary.

Specification Table

- Table list all specifications of this PLL and point out which need to measured.

Item	Specification (unit)	measure
Vdd (Supply voltage)	3.3 V	N/A
Kvco	60 MHz/V	Yes
Phase Noise	-98 dBc @ 1MHz	Yes
Locking time	22 us	Yes
Jitter	430 ps	Yes
Power Consumption	11 mW	Yes
Chip Area	1500 X 1500 um^2	N/A
…..		

Measured Considerations

- List all measured instruments you need, and illustrate those purpose.
- List measure setup for each parameter you need to know.
- Mark where you will measure.
  (in TSRI, self's Lab., et al.…)

References

- [1] Donhee Ham, Ali Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," IEEE Journal of Solid-State Circuits, Vol. 36 No.6, pp.896-909, June 2001.
- [2] ….