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Tape-out Review Form (*for Cell-based IC*)

The Tape-out Review Form is intended to remind designers to demonstrate design concepts and comprehend design, simulation, layout verification, and tape-out notes. It is hoped that the success rate of IC design and comprehensive learning results can be improved. As a result, the adviser and designer are asked to double-check that the requirements in this form were noted during the chip design process and that the signature was affixed after confirming the filling. If the design content and completion of the Tape-out Review Form are found to be inconsistent during review, the chip tape-out manufacturing qualifications will most likely be canceled. Refer to the cell-base example on the TSRI website and fill out the form honestly.

1. IC Design Case Content

1-1 The GDS file name uploaded to the tape-out electronic webpage: CHIP.gds

1-2 Name of Top Cell: CHIP

1-3 What category does need design fall under:
- ■ Exclusively a digital circuit design (the layout file has no full-custom design block.)
- □ Mixed signal circuit design (the layout file has a full-custom design block.)

1-4 Project name: ***a low-power RSA decoder/encoder and interface circuit***

1-5 Maximum work frequency: **200MHz**

How many clock domains are there in this design case:

The clock operational frequencies of respective clock domains are: **CLK1: 200MHz CLK2: 50MHz**

1-6 Power consumption: ***50mW***

1-7 Chip area: ***1500 um*** X ***1500 um***

1-8 Name of process used:

- □ TSMC 0.35 UM Mixed-Signal 2P4M Polycide 3.3/5V
  (Please complete Question 2 as well as Question 10 to Question 17)
- □ TSMC 0.18UM CMOS HIGH VOLTAGE MIXED SIGNAL BASED GENERATION II BCD 1P6M SALICIDE AL_FSG 1.8/ 5/ 6/ 7/ 8/ 12/ 16/ 20/ 24/ 29/ 36/ 45/ 55/ 65/ 70V/ VG1.8/ 5V AND 5/ 6/ 7/ 8/ 12/ 16/ 20/ 24/ 29/ 36/ 45/ 55/ 65/ 70V/ VG5V
  (Please complete Question 3 as well as Question 10 to Question 17)
- □ TSMC 0.18 UM CMOS Mixed Signal RF General Purpose MiM Al 1P6M 1.8&3.3V
  (Please complete Question 4 as well as Question 10 to Question 17)
- ■ TSMC 90 nm CMOS Mixed Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0&3.3V (With UTM)
  (Please complete Question 5 as well as Question 10 to Question 17)
- □ TSMC 40 nm CMOS LOGIC General Purpose Superb (40G) ELK Cu 1P10M 0.9/2.5V
  (Please complete Question 6 as well as Question 10 to Question 17)
- □ TSMC 28 nm CMOS RF High Performance Compact Mobile Computing Plus ELK Cu 1P10M 0.9/2.5V
  (Please complete Question 7 as well as Question 10 to Question 17)
- □ TSMC 16 nm CMOS LOGIC FinFET Compact(Shrink) LL ELK Cu 1P13M 0.8/1.8V

(Please complete Question 8 as well as Question 10 to Question 17)

□ UMC 0.18um Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process

(Please complete Question 9 to Question 17)

2. TSMC 0.35 UM Mixed-Signal 2P4M Polycide 3.3/5V tape-out notes

2-1 Is the core library used? □ Yes □ No

2.1.1 Name of the core library used: □ CBDK_TSMC035_TSMC_v7.0 □ other_____

※ Notes: Refer to cad/CBDK/CBDK035_TSMC_TSMC/01_rev.txt for the version used.

2.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

2.1.3 Is there filling using core filler? □ Yes □ No

2-2 Is the IO library used? □ Yes □ No

2.2.1 Name of IO library used: □ CBDK035_TSMC_TSMC_v7.0 □ D35/IOPAD_STC □other_____

※ Note 1: CBDK035_TSMC_TSMC_v7.0 is sourced from **/cad/CBDK/CBDK035_TSMC_TSMC**.

※ Note 2: D35/IOPAD_STC is sourced from **/cad/PDK/D35/IOPAD_STC**.

(2.3.2 to 2.3.5) below only needs to be filled out by the CBDK035_TSMC_TSMC_v7.0 IO library user.

2.2.2 Is IO filler added? □ Yes □No

2.2.3 Is a bonding pad added? □ Yes □ No

2.2.4 Is the addTagCell option checked on the tape-out electronic webpage: □ Yes □ No

2.2.5 Is R0 the cell's placement direction in the lower left corner? □ Yes □ No

2-3 Filling of dummy pattern

2.3.1 If the design is exclusively a digital circuit design, the TSRI will fill out the dummy pattern after the layout is replaced. Has the information provided above been verified? □Yes □No

2.3.2 If the layout file is a mixed-signal design, the full-custom design block must independently fill the dummy pattern and select unfilled image layers, including the block layer of Layer FUSE [FW(235)]. The TSRI will fill out the dummy pattern once the layout of the cell-based design block has been replaced. Has the information provided above been verified? □ Yes □ No

2.3.3 Has the addDummyCell option on the tape-out electronic webpage been selected, and has the TSRI filled out the dummy patern? □ Yes □ No

2-4 DRC verification

2.4.1 In this design case, has the DRC verification of the queue server been completed? □ Yes □ No

2.4.2 The name of the DRC verification result file after queue server replacement:

_____

2.4.3 Has the DRC verification file been uploaded to the tape-out electronic webpage after the queue server was replaced? □ Yes □ No

2.4.3.1 The DRC file name uploaded to the tape-out electronic webpage:_____

2.4.3.2 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

2.4.4 Does the queue server's completed DRC result content contain DRC-deviated errors? □ Yes □ No

※ Refer to the following for content details: http://www2.cic.org.tw/~shuttle/drc/all/D35.pdf.

	DRC error type	Notes

□	RPO.S.3	This process does not provide high resistance Poly2.
□	LATI.2	This error is only disregardable when it manifests in resistance. Should this occur on crystals, it is necessary to rectify this error.
□	OFFGRID	
□	□ AMS.1.M1 □ AMS.1.M2 □ AMS.1.M3 □ AMS.1.M4	AMS series errors are only disregardable when they manifest on TSMC I/O PAD. After executing the DRC of whole chips, please thoroughly examine if AMS series errors appear in the core or the junction between the core and I/O PAD.
□	□ CB.R.1~4 □ CB.C.1~2 □ CB.S.1~4 □ CB.E.1~12 □ CB.W.1~4	As a result of RF and other wiring requirements, the passivation issue is not currently error-free, as determined by a discussion between the CIC and senior engineers who are actively involved in processes. Please, however, follow CB series rules as much as possible to ensure the feasibility and success of wire bonding.
□	□ NW.W.2 □ NW.S.1 □ CO.E.1 □ CB.E.5, CB.E.7, and CB.E.9	The allowable DRC errors of STC 3.3V I/O PAD: ➢ NW.W.2 errors occur in VDDI_33, VDDE_33, VSSI_33, and AIN_33. ➢ NW.S.1 errors occur in VDDI_33, VDDE_33, VSSI_33, and AIN_33. ➢ CO.E.1 errors occur in BI33_XX and DIN_33. ➢ CB.E.5, CB.E.7, and CB.E.9 occur in all pads.
□	□ NW.W.2 □ NW.S.1 □ CO.E.1 □ CB.E.5, CB.E.7, and CB.E.9	The allowable DRC errors of STC 5V I/O PAD: ➢ NW.W.2 errors occur in C_VDDI, C_VDDE, C_VSSI, and AIN_05. ➢ NW.S.1 errors occur in C_VDDI, C_VDDE, C_VSSI, and AIN_05. ➢ CO.E.1 errors occur in BI05_XX and DIN05_01. ➢ CB.E.5, CB.E.7, and CB.E.9 occur in all pads.
□	NET_AREA_RATIO_RDBS	
□	□ PO.R.1 □ M1.R.1 □ M2.R.1 □ M3.R.1 □ M4.R.1	The errors are only allowed in destiny errors that still occur in the CBDK circuit after the addDummy command.

2-5 LVS verification

2.5.1 Are there any LVS errors in this design case before completing DRC verification on the queue server? □ Yes □ No

2.5.2 Is there a blackbox not provided by CIC? □ Yes □ No

2.5.3 What is the name of the verification LVS software used? □ Calibre LVS □ _____

2.5.4 The LVS verification file name uploaded to the tape-out electronic webpage:_____

2.5.5 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

2.5.6 Please verify the DRC verification result file on the queue server, especially the lvs.rep.ext file content in the Short_Check_With_Dummy data, to see if a lvs.rep.short file appears, or if there are any other LVS errors or warning messages relating to signal short circuits: □ Yes □ No

Notes: Through the online post-layout transistor level simulation on the queue server, the designer can self-verify whether the error occurrence affects the circuit design function.

3. TSMC 0.18UM CMOS HIGH VOLTAGE MIXED SIGNAL BASED GENERATION II BCD 1P6M SALICIDE AL_FSG 1.8/ 5/ 6/ 7/ 8/ 12/ 16/ 20/ 24/ 29/ 36/ 45/ 55/ 65/ 70V/ VG1.8/ 5V AND 5/ 6/ 7/ 8/ 12/ 16/ 20/ 24/ 29/ 36/ 45/ 55/ 65/ 70V/ VG5V tape out notes.

3-1 Is the core library used? □ Yes □ No

3.1.1 Name of the core library used: □ CBDK_T18HVG2_ARM_v4.0 □ other_____

※Notes: Refer to /cad/ CBDK/CBDK_T18HVG2_ARM/01_rev.txt for the version used.

3.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

3.1.3 Is there filling using core filler? □ Yes □ No

3-2 Filling of dummy pattern

3.2.1 If the design is exclusively a digital circuit design, the TSRI will fill out the dummy pattern after the layout is replaced. Has the information provided above been verified? □Yes □No

3.2.2 If the layout file is a mixed-signal design, the full-custom design block must independently fill the dummy pattern and select unfilled image layers, including the Layer DMEXCL (Layer number 150; Data type 1~6), Layer ODBLK (Layer number 150; Data type 20), and Layer POBLK (Layer number 150; the block layer of Data type 21), eight Layers in all; after the layout is replaced in the cell-based design block the TSRI will fill out the dummy pattern. Has the information provided above been verified? □Yes □No

3.2.3 Has the addDummyCell option on the tape-out electronic webpage been selected, and has the TSRI filled out the dummy patern? □ Yes □ No

3-3 DRC verification

3.3.1 This process must be approved by the verification of three DRC rules:

(1) /cad/PDK/T18HVG2/T18HVG2_DRC.rule

(2) /cad/PDK/T18HVG2/T18HVG2_ANTENNA.rule

(3) /cad/PDK/T18HVG2/T18HVG2_WireBond.rule

Has the above verification process granted approval? □ Yes □ No

3.3.2 In this design case, has the DRC verification of the queue server been completed? □ Yes □ No

3.3.3 The name of the DRC verification result file after queue server replacement:

_____

3.3.4 Has the DRC verification file been uploaded to the tape-out electronic webpage after the queue server was replaced? □ Yes □ No

3.3.4.1 The DRC file name uploaded to the tape-out electronic webpage:_____

3.3.4.2 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

3.3.5 Does the queue server's completed DRC result content contain DRC-deviated errors? □ Yes □ No

※ **Refer to the following for content details: http://www2.cic.org.tw/~shuttle/drc/all/T18HVG2.pdf**

	DRC error type	Causes of DRC errors	Notes
□	DRM.R.1		Please refer to the related explanations in process document T-018-CV-DR-027 before disregarding it.
□	MOM.R.2		The MOM capacitance can be disregarded if it is not used in the design.
□	DOD.R.1		If OD is used to fill the density, it can be disregarded.

3-4 LVS verification

3.4.1 Are there any LVS errors in this design case before completing DRC verification on the queue server? □ Yes □ No

3.4.2 Is there a blackbox not provided by CIC? □ Yes □ No

3.4.3 What is the name of the verification LVS software used? □ Calibre LVS □ _____

3.4.4 The LVS verification file name uploaded to the tape-out electronic webpage:_____

3.4.5 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

3.4.6 Please verify the DRC verification result file on the queue server, especially the lvs.rep.ext file content in the Short_Check_With_Dummy data, to see if a lvs.rep.short file appears, or if there are any other LVS errors or warning messages relating to signal short circuits: □ Yes □ No

Notes: Through the online post-layout transistor level simulation on the queue server, the designer can self-verify whether the error occurrence affects the circuit design function.

4. TSMC 0.18 UM CMOS Mixed Signal RF General Purpose MiM Al 1P6M 1.8&3.3V tape-out notes

4-1 Is the core library used? □ Yes □ No

4.1.1 Name of the core library used: □ CBDK_TSMC018_Arm_v4.0 □ other_____

※ Note: Refer to /cad/ CBDK/CBDK_TSMC018_Arm/01_rev.txt for the version used.

4.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

4.1.3 Is there filling using core filler? □ Yes □ No

4-2 Is the memory used? □ Yes □ No

	Type	Upload the name of the spec file (*.spec) and the file name of the corresponding ROM burning (*.txt).	Memory size	Quantity
■Example	t18rodsd (ROM)	(1) ROMexample1.spec (ROMexample1.txt) (2) ROMexample2.spec (ROMexample2.txt)	(1) 256 X 4 (2) 1024 X 8	1 1
□	t18rodsd (ROM)			
□	t18ra1shd			
□	t18ra2sh			
□	t18rf1sh			
□	t18rf2sh			

4.2.1 Verify if the information filled out matches the information on the tape-out electronic webpage: □ Yes □ No

4.2.2 Is the burning data produced in a UNIX or LINUX work station and generated by the vi editor? (it is recommended that the vi editor be used to generate burning data files; otherwise, problems may arise when generating ROM.): □ Yes □ No

4-3 Is the IO library used? □ Yes □ No

4.3.1 Name of IO library used: □ T018MMIO001 □ CBDK_TSMC018_Arm_v4.0 □ other_____

4.3.2 Is IO filler added? □ Yes □ No

4.3.3 Is a bonding pad added? □ Yes □ No

Below (C-1 to C-3) only need to be filled out by CBDK_TSMC018_Arm_v4.0 IO library users.

C-1. : Is there only one VDD2POC power pad in every power domain? □ Yes □ No

C-2. : Is the addTagCell option checked on the tape-out electronic webpage: □ Yes □ No

C-3. : Is R0 the cell's placement direction in the lower left corner? □ Yes □ No

4-4 Filling of dummy pattern

4.4.1 If the design is exclusively a digital circuit design, the TSRI will fill out the dummy pattern after the layout is replaced. Has the information provided above been verified? □Yes □No

4.4.2 If the layout file is a mixed-signal design, the full-custom design block must independently fill the dummy pattern and select unfilled image layers, including the Layer DMEXCL (Layer number 150;

Data type 1~6), Layer ODBLK (Layer number 150; Data type 20), and Layer POBLK (Layer number 150; the block layer of Data type 21), eight Layers in all; after the layout is replaced in the cell-based design block the TSRI will fill out the dummy pattern.

Has the information provided above been verified? □Yes □No

4.4.3 Has the addDummyCell option on the tape-out electronic webpage been selected, and has the TSRI filled out the dummy patern? □ Yes □ No

4-5 DRC verification

4.5.1 In this design case, has the DRC verification of the queue server been completed? □ Yes □ No

4.5.2 The name of the DRC verification result file after queue server replacement:

_____

4.5.3 Has the DRC verification file been uploaded to the tape-out electronic webpage after the queue server was replaced? □ Yes □ No

4.5.3.1 The DRC file name uploaded to the tape-out electronic webpage:_____

4.5.3.2 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

4.5.4 Does the queue server's DRC result content contain DRC-deviated errors? □ Yes □ No

※ **Refer to the following for content details: http://www2.cic.org.tw/~shuttle/drc/all/T18.pdf.**

TSMC18 List of DRC-deviated Errors			
□ VIA2.E.3	□ LUP.1g	□ LUP.2g	□ DRM.R.1
□ OD.R.1	□ NET_AREA_RATIO_RDBS	□ FPAD.R.1	□ NW.R.1
□ DRM.R.1	□ DOD.DN.1	□ DOD.DN.2	□ UTM20K.C.1
□ UTM20K.E.3	□ UTM20K.I.1	□ CTM.R.2	
The following errors can only be deviated from within the I/O Pad range.			
□ LUP.4g	□ LUP.5.3g_3.3V		
The following errors can only be deviated from within the core circuit range.			
□ VIA3.E.3	□ VIA4.E.3		
The following errors can only be deviated on the digital pad provided by TSRI.			
□ RES.2	□ RES.4_PO	□ RES.8	□ NW.S.1.1
□ ESD.24g	□ LUP.5.3g_3.3V	□ ESD.28g	□ ESD.34g
□ ESD.25g			
Other DRC-deviated errors			
□ Density	Please use the dummy filling program to perform filling. Errors can be disregarded after filling.		
□ OD.EX.1	Those that occur on the I/O pad and the TSRI memory can be disregarded.		

TSMC18 List of Density DRC-deviated errors		
□ NO.IND.OD.R.1	□ NO.IND.PO.R.3	□ NO.IND.M1.R.1
□ NO.IND.M2.R.1	□ NO.IND.M3.R.1	□ NO.IND.M4.R.1
□ NO.IND.M5.R.1	□ UTM20K.R.1	

TSMC18 List of Other DRC-deviated Errors	
※ **Attention: If there are errors that CIC does not allow, this case will not be allowed to tape out.**	
DRC error number	Causes of DRC errors

4-6 LVS verification

4.6.1 Are there any LVS errors in this design case before completing DRC verification on the queue server? □ Yes □ No

4.6.2 Is there a blackbox not provided by CIC? □ Yes □ No

4.6.3 What is the name of the verification LVS software used? □ Calibre LVS □ _____

4.6.4 The LVS verification file name uploaded to the tape-out electronic webpage:_____

4.6.5 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

4.6.6 Please verify the DRC verification result file on the queue server, especially the lvs.rep.ext file content in the Short_Check_With_Dummy data, to see if a lvs.rep.short file appears, or if there are any other LVS errors or warning messages relating to signal short circuits: □ Yes □ No

Notes: Through the online post-layout transistor level simulation on the queue server, the designer can self-verify whether the error occurrence affects the circuit design function.

5. TSMC 90 nm CMOS Mixed Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0&3.3V (With UTM) tape-out notes

5-1 Is the core library used? ■ Yes □ No

5.1.1 Name of the core library used: ■ CBDK_TSMC90GUTM_Arm_v1.2 □ other_____

※ Note: Refer to /cad/ CBDK/CBDK_TSMC90GUTM_Arm_v1.2/01_rev.txt for the version used.

5.1.2 Has the cell name been changed? □ Yes ■ No (It is advised not to change the cell name.)

5.1.3 Is multi-Vt used for core cells? ■ Yes □ No

5.1.4 What type of core cell is used? ■ RVT ■ HVT

5.1.5 Is the core filler filled? ■ Yes □ No

5-2 Is the memory used? ■ Yes □ No

	Type	Upload the name of the spec file (*.spec) and the file name of the corresponding ROM burning (*.txt).	Memory size	Quantity
■ Example	t90utm_rodsd (ROM)	(1) ROMexample1.spec (ROMexample1.txt) (2) ROMexample2.spec (ROMexample2.txt)	(1) 256 X 4 (2) 1024 X 8	1 1
■	t90utm_rodsd	t90utm_rodsd.spec(ROMt90utm_rodsd.txt)	128 X 8	1
■	t90utm_sram_sp_adv	t90utm_sram_sp_adv.spec	512 X 8	1
□	t90utm_sram_dp_adv			
□	t90utm_rf_sp_adv			
□	t90utm_rf_dp_adv			

5.2.1 Verify if the information filled out matches the information on the tape-out electronic webpage: ■ Yes □ No

5.2.2 Is the burning data produced in a UNIX or LINUX work station and generated by the vi editor? (it is recommended that the vi editor be used to generate burning data files; otherwise, problems may arise when generating ROM.): ■ Yes □ No

5-3 Is the IO library used? ■ Yes □ No

5.3.1 Name of IO library used: ■ CBDK_TSMC90GUTM_Arm_v1.2 □ other_____

5.3.2 Is there only one PVDD2POC_33 power pad in every power domain? ■ Yes □ No

5.3.3 Is IO filler added? ■ Yes □ No

5.3.4 Is a bonding pad added? ■ Yes □ No

5.3.5 Is the addTagCell option checked on the tape-out electronic webpage: ■ Yes □ No

5.3.6 Is R0 the cell's placement direction in the lower left corner? ■ Yes □ No

5-4 Is ADPLL IP provided by CIC used? ■ Yes □ No

5.4.1 What is the ADPLL IP version used? ■ ADPLL_TSMC90GUTM_CIC_v1.0

5-5 Is CPU IP provided by CIC used? □ Yes ■ No (If yes, fill out Item 16.)

5.5.1 What type of CPU is used? □ AndesCore

5-6 Filling of dummy pattern

5.6.1 If the design is exclusively a digital circuit design, the TSRI will fill out the dummy pattern after the layout is replaced. Has the information provided above been verified? ■ Yes □ No

5.6.2 If the layout file is a mixed-signal design, the full-custom design block must independently fill the dummy pattern and select unfilled image layers, Layer DMEXCL (Layer number 150; Data type 1~9), Layer ODBLK (Layer number 150; Data type 20) Layer POBLK (Layer number 150; and the block layer of Data type 21), 11 layers in total; after the layout is replaced in the cell-based design block the TSRI will fill out the dummy pattern. Has the information provided above been verified? ■ Yes □ No

5.6.3 Has the addDummyCell option on the tape-out electronic webpage been selected, and has the TSRI filled out dummy pattern? ■ Yes □ No

5-7 DRC verification

5.7.1 Related allowable DRC errors are attached in CBDK_ TSMC90GUTM_Arm_v1.2 ″KNOWN PROBLEMS AND LIMITATIONS.txt″. Has this file been verified before uploading? ■ Yes □ No

5.7.2 In this design case, has the DRC verification of the queue server been completed? ■ Yes □ No

5.7.3 The name of the DRC verification result file after queue server replacement:

18-3-9_cic01c_DRC_10700

5.7.4 Has the DRC verification file been uploaded to the tape-out electronic webpage after the queue server was replaced? ■ Yes □ No

5.7.4.1 The DRC file name uploaded to the tape-out electronic webpage: DRC.rep

5.7.4.2 Does the file uploaded to the electronic tape-out webpage match the information filled out above? ■ Yes □ No

5.7.5 Does the queue server's DRC result content contain DRC-deviated errors? ■ Yes □ No

	DRC error type	Notes
■	Mx.DN.2	(**x=1~8**) If the area uses dummy generation to fill the density, it can be disregarded.
■	Mx.DN.1_Mx.DN.3:H	
□	Mx.DN.1_Mx.DN.3:L	
□	PO.DN.2	
□	OD.DN.2_OD.DN.3:H_IO	
□	OD.DN.2_OD.DN.3:H_CORE	
□	OD.DN.2_OD.DN.3:L	
□	UTM.DN.1:H	
□	UTM.DN.1:L	

□	Mx.DN.5	The metal density of three consecutive layers in CBM is less than 15% within (**x=1~5**). Please keep in mind that if this rule is not followed, the MIM capacitance characteristics may suffer. Please evaluate and make changes or disregard it.
□	Mn.DN.5:L	When using MIM capacitance and the M8 density in CTMDMY is less than 50%, keep in mind that failure to follow this rule may have an effect on MIM capacitance characteristics. Please reconsider and make changes, or ignore it.
■	UTM.DN.5R	If the INDDMY exceeds 5% of the chip area, it can be disregarded.
□	AP.DN.1:L	TP does not need to be supplemented with density and can be disregarded.

TN90GUTM List of Other DRC-deviated Errors	
※ **Attention: If there are errors other than the above-mentioned, make corrections; otherwise this case will not be allowed to tape out. Refer to the following for content details: http://www2.cic.org.tw/~cis/chipapply/doc/handout.pdf.**	
DRC error number	Causes for DRC-deviated Errors

5-8 LVS verification

5.8.1 Are there any LVS errors in this design case before completing DRC verification on the queue server? □ Yes ■ No

5.8.2 Is there a blackbox not provided by CIC? □ Yes ■ No

5.8.3 What is the name of the verification LVS software used? ■ Calibre LVS □ _____

5.8.4 The LVS verification file name uploaded to the tape-out electronic webpage: lvs.rep

5.8.5 Does the file uploaded to the electronic tape-out webpage match the information filled out above? ■ Yes □ No

5.8.6 Please verify the DRC verification result file on the queue server, especially the lvs.rep.ext file content in the Short_Check_With_Dummy data, to see if a lvs.rep.short file appears, or if there are any other LVS errors or warning messages relating to signal short circuits: □ Yes ■ No

Notes: Through the online post-layout transistor level simulation on the queue server, the designer can self-verify whether the error occurrence affects the circuit design function.

6. TSMC 40 nm CMOS LOGIC General Purpose Superb (40G) ELK Cu 1P10M 0.9/2.5V tape-out notes

6-1 Is the core library used? □ Yes □ No

6.1.1 Name of the core library used: □ CBDK_TSMC40_core_Arm_v2.0 □ CBDK_TN40G_ITRI_v3.1 □ Other_____

6.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

6.1.3 Is multi-Vt used for core cells? □ Yes □ No

6.1.4 What type of core cell is used? □ LVT □ RVT □ HVT

6.1.5 Is there filling using core filler? □ Yes □ No

6-2 Is the memory used? □ Yes □ No

	Type	Memory size	Quantity
■Example	rf_2p_hse_rvt_hvt_rvt	(1) 256 X 4 (2) 1024 X 8	1 1
□	rf_2p_hse_rvt_hvt_rvt		

□	rom_via_rvt_hvt_rvt		
□	sram_sp_hde_rvt_hvt_rvt		
□	sram_dp_hde_rvt_hvt_rvt		
□	rf_sp_hde_rvt_hvt_rvt		

6.2.1 Has the memory been correctly replaced into the actual layout? □ Yes □ No

6-3 Is the IO library used? □ Yes □ No

6.3.1 Name of IO library used: □ CBDK_TSMC40_io_TSMC_v2.0 □ other _____

6.3.2 Is there only one VDD2POC power pad in every power domain? □ Yes □ No

6.3.3 Is IO filler added? □ Yes □ No

6.3.4 Is a bonding pad added? □ Yes □ No

6.3.5 Is the addTagCell option checked on the tape-out electronic webpage: □ Yes □ No

6.3.6 Is R0 the cell's placement direction in the lower left corner? □ Yes □ No

6-4 Filling of dummy pattern

6.4.1 If the design is exclusively a digital circuit design, the TSRI will fill out the dummy pattern after the layout is replaced. Has the information provided above been verified? □Yes □No

6.4.2 If the layout file is a mixed-signal design, the full-custom design block must independently fill the dummy pattern and select unfilled image layers, including Layer DMEXCL (Layer number 150; Data type 1~9), Layer ODBLK (Layer number 150; Data type 20) and Layer POBLK (Layer number 150; the block layer of Data type 21), 11 layers in total; after the layout is replaced in the cell-based design block, the TSRI will fill out the dummy pattern. Has the information provided above been verified? □Yes □No

6.4.3 Has the addDummyCell option on the tape-out electronic webpage been selected, and has the TSRI filled out the dummy patern? □ Yes □ No

6-5 DRC verification

6.5.1 Does the queue server's DRC result content contain DRC-deviated errors? □ Yes □ No

	DRC error type	Notes
□	LUP5.4.1	The error can only occur in the IO library.
□	DTCD.DN.2	Large chip areas can be disregarded.
□	MOM.R.2	The MOM capacitance can be disregarded if it is not used in the design.
□	DRM.R.1	This information is only provided as a reminder of the importance of inspecting wirebond rules and antenna rules, which can be disregarded.
□	RM.WARN.4:M1	This error can only appear in the IOPAD of PVDD3AC.
□	RM.WARN.4:M2	This error can only appear in the IOPAD of PVDD3AC.

6.5.2 In general, the design case in this process does not allow concurrences of any DRC error other than those listed in 6.5.1.

TN40G List of Other DRC-deviated Errors	
※ **Attention: For DRC errors in this area, contact a TN40G process engineer to report and file an application; otherwise, the errors will be considered deviated from DRC verifications, and tape-out is not recommended.**	
DRC error number	Causes for DRC-deviated Errors

6-6 LVS verification

6.6.1 Are there LVS errors in this design case? □ Yes □ No

6.6.2 Is there a blackbox not provided by CIC? □ Yes □ No

6.6.3 Name of verification LVS software used: □ Calibre LVS □ _____

6.6.4 The LVS verification file name uploaded to the tape-out electronic webpage: _____

6.6.5 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

7. TSMC 28 nm CMOS RF High Performance Compact Mobile Computing Plus ELK Cu 1P10M 0.9/2.5V tape-out notes

7-1 Is the core library used? □ Yes □ No

7.1.1 Name of the core library used: □ CBTK_TSMC28HPCPlus_core_TSMC_v1.0 □ other_____

7.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

7.1.3 Is multi-Vt used for core cells? □ Yes □ No

7.1.4 What type of core cell is used? □ LVT □ RVT □ HVT

7.1.5 Is there filling using core filler? □ Yes □ No

7.1.6 Is the well tap cell filled: (Cell Name: TAPCELLBWP12T30P140): □ Yes □ No

7.1.7 Is the end cap cell filled?

(Cell Name: BOUNDARY_LEFTBWP12T30P140, BOUNDARY_RIGHTBWP12T30P140): □ Yes □ No

7.1.8 Have the core cell and core filler been correctly replaced into the actual layout? □ Yes □ No

7-2 Is the memory used? □ Yes □ No

	Type	Memory size	Quantity
■Example	TN28HPCPlus One Port Register File	(1) 256 X 4 (2) 1024 X 8	1 1
□	TN28HPCPlus One Port Register File		
□	TN28HPCPlus Two Port Register File		
□	TN28HPCPlus Single Port SRAM		
□	TN28HPCPlus Dual Port SRAM		
□	TN28HPCPlus Ultra High Density Single Port SRAM		
□	TN28HPCPlus Ultra High Density Dual Port SRAM		
□	TN28HPCPlus ROM		

7-3 Is the IO library used? □ Yes □ No

7.3.1 Name of IO library used: □ CBTK_TSMC28HPCPlus _io_TSMC_v1.0 □ other_____

7.3.2 Is there only one PVDD2POC_H_G power pad and one PVDD2POC_V_G power pad in every power domain? □ Yes □ No

7.3.3 Is IO filler added? □ Yes □ No

7.3.4 Is a bonding pad added? □ Yes □ No

7.3.5 Have the IO pad, IO filler, and bonding pad been correctly replaced into the actual layout? □ Yes □ No

7.3.6 Has an L-shaped corner tag been added to the chip's left lower corner as instructed? □ Yes □ No

7-4 DRC verification

7.4.1 In general, the design case in this process does not allow concurrences of any DRC errors.

TN28HPCplu List of Other DRC-deviated Errors

※ **Attention: For DRC errors in this area, contact a TN28HPCplu process engineer to report and file an application; otherwise, the errors will be considered deviated from DRC verifications, and tape-out is not recommended.**	
DRC error number	Causes for DRC-deviated Errors

7-5 LVS verification

7.5.1 Are there LVS errors in this design case? □ Yes □ No

7.5.2 Name of verification LVS software used: □ Calibre LVS □ _____

7.5.3 Uploaded LVS verification file name: _____

7.5.4 Is the uploaded file the same as the information entered above? □ Yes □ No

8. TSMC 16 nm CMOS LOGIC FinFET Compact(Shrink) LL ELK Cu 1P13M 0.8/1.8V tape-out notes

8-1 Is the core library used? □ Yes □ No

8.1.1 Name of the core library used: □ CBTK_TSMC16FFC_core_TSMC_v1.0: □ other_____

8.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

8.1.3 Is multi-Vt used for core cells? □ Yes □ No

8.1.4 What type of core cell is used? □ SVT □ LVT □ ULVT □ ILVT

8.1.5 Is there filling using core filler? □ Yes □ No

8.1.6 Is the well tap cell filled: (Cell Name: TAPCELLBWP16P90: □ Yes □ No

8.1.7 Is the end cap cell filled? (Cell name: BOUNDARY_PTAPBWP16P90, BOUNDARY_NTAPBWP16P90): □ Yes □ No

8.1.8 Have the core cell and core filler been correctly replaced into the actual layout? □ Yes □ No

8-2 Is the memory used? □ Yes □ No

	Type	Memory size	Quantity
■Example	TN16FFC Low Leakage One Port Register File	(1) 256 X 4 (2) 1024 X 8	1 1
□	TN16FFC Low Leakage One Port Register File		
□	TN16FFC Low Leakage Two Port Register File		
□	TN16FFC Low Leakage Dual Port SRAM		
□	TN16FFC Low Leakage High Density Single Port Multi Bank SRAM		
□	TN16FFC Low Leakage High Density Single Port Single Bank SRAM		
□	TN16FFC Low Leakage Read Only Memory		
□	TN16FFC Low Leakage Smaller High Current Single Port Single Bank SRAM		
□	TN16FFC Low Leakage Smaller High Density Single Port Multi Bank SRAM		
□	TN16FFC Low Leakage Smaller High Density Single Port Single Bank SRAM		
□	TN16FFC Low Leakage Single Port SRAM		
□	TN16FFC Low Leakage Ultra High Density One Port Register File		
□	TN16FFC Low Leakage Ultra High Density Two Port Register File		

8-3 Is the IO library used? □ Yes □ No

8.3.1 Name of the core library used: □ CBTK_TSMC16FFC_io_TSMC_v1.0 □ other_____

8.3.2 Is there only one PVDD2POCM power pad in every power domain? □ Yes □ No

8.3.3 Is there at least one PCBRTE power pad in every power domain? □ Yes □ No

8.3.4 Is IO filler added? □ Yes □ No

8.3.5 Is a bonding pad added? □ Yes □ No

8.3.6 Have the IO pad, IO filler, and bonding pad been correctly replaced into the actual layout? □ Yes □ No

8.3.7 Has an L-shaped corner tag been added to the chip's left lower corner as instructed? □ Yes □ No

8-4 DRC verification

8.4.1 In general, the design case in this process does not allow concurrences of any DRC errors.

TN16FFC List of Other DRC-deviated Errors	
※ **Attention: For DRC errors in this area, contact a TNFFC process engineer to report and file an application; otherwise, the errors will be considered deviated from DRC verifications, and tape-out is not recommended.**	
DRC error number	Causes for DRC-deviated Errors

8-5 LVS verification

8.5.1 Are there LVS errors in this design case? □ Yes □ No

8.5.2 What is the name of the verification LVS software used? □ Calibre LVS □ _____

8.5.3 Uploaded LVS verification file name:_____

8.5.4 Is the uploaded file the same as the information entered above? □ Yes □ No

9. UMC 0.18um Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process tape-out notes

9-1 Is the core library used? □ Yes □ No

9.1.1 Name of the core library used: □ CBDK018_UMC_Faraday_v1.0 □CBDK_UMC018_ITRI_v0.8 □ Other_____

9.1.2 Has the cell name been changed? □ Yes □ No (It is advised not to change the cell name.)

9.1.3 Is there filling using core filler? □ Yes □ No

9-2 Is the memory used? □ Yes □ No

	Type	Upload the name of the spec file (*.spec) and the file name of the corresponding ROM burning (*.txt).	Memory size	Quantity
■ Example	u18mem (RAM)	(1) RAMexample1.spec (RAMexample1.txt) (2) RAMexample2.spec (RAMexample2.txt)	(1) 256 X 4 (2) 1024 X 8	1 1
□	u18mem			

9.2.1 Verify if the information filled out matches the information on the tape-out electronic webpage: □ Yes □ No

9.2.2 Is the burning data produced in a UNIX or LINUX work station and generated by the vi editor? (it is recommended that the vi editor be used to generate burning data files; otherwise, problems may arise when generating ROM.): □ Yes □ No

9-3 Is the IO library used? □ Yes □ No

9.3.1 Name of IO library used: □ CBDK_UMC18_Faraday □ CBDK_UMC018_ITRI □ other_____

9.3.2 Is IO filler added? □ Yes □ No

9.3.3 Is a bonding pad added? □ Yes □ No

Below (C-1 to C-2) only need to be filled out by CBDK_UMC18_Faraday IO library or CBDK_UMC018_ITRI IO Library users.

C-1. : Is the addTagCell option checked on the tape-out electronic webpage: □ Yes □ No

C-2. : Is R180 the cell's placement direction in the lower left corner? □ Yes □ No

9-4 Filling of dummy pattern

9.4.1 If the design is exclusively a digital circuit design, the IMC will fill in the dummy pattern. According to the Diffusion/Poly/Metal Density Rules, the filled dummy patterns include Diffusion/Poly/Metal 1–6 Dummy. Has the information provided above been verified? □Yes □No

9.4.2 If the layout file is a mixed-signal design, the full-custom design block must independently fill the dummy pattern, and the Dummy Block Layer of the GDS No 70~77 Data Type 1 must be added to the outer frame, eight layers in total. This is to avoid affecting circuit characteristics as a result of the dummy pattern in the full-custom flow area. For Cell-Based Flow region, Diffusion/Poly/Metal Dummy will be filled in by UMC. Has the information provided above been verified? □Yes □No

9-5 DRC verification

9.5.1 In this design case, has the DRC verification of the queue server been completed? □ Yes □ No

9.5.2 The name of the DRC verification result file after queue server replacement:

_____

9.5.3 Has the DRC verification file been uploaded to the tape-out electronic webpage after the queue server was replaced? □ Yes □ No

9.5.3.1 The DRC file name uploaded to the tape-out electronic webpage:_____

9.5.3.2 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

9.5.4 Does the queue server's DRC result content contain DRC-deviated errors? □ Yes □ No

※ **Refer to the following for content details: http://www2.tsri.org.tw/~shuttle/drc/all/U18.pdf.**

UMC18 List of DRC-deviated errors			
□ RECOMMEND_4.14 L	□ 4.1M	□ 4.20G	□ 4.22G
□ 4.24G	□ 4.26G	□ 4.28G	□ 4.31F
□ 4.20C	□ 4.22C	□ 4.24C	□ 4.26C
□ 4.28C	□ 4.29NOTICE	□ 4.01Z.NO_IND_OD	□ 4.14Z.NO_IND_PO1
□ 4.20F.NO.IND_M1	□ 4.22F.NO_IND_M2	□ 4.24F.NO_IND_M3	□ 4.26F.NO_IND_M4
□ 4.28F.NO_IND_M5	□ 4.31E.NO_IND_M6	□ 6Bb.ME1	□ Sanity_1
□ IO5.1.W2	□ IO5.1.R1	□ IO5.2.1.W1.a	□ IO5.2.1.W1.b
□ IO5.2.2.L1.a	□ IO5.2.2.L1.c	□ IO5.5.4.Note	□ Latch.4.1
□ Latch.4.2	□ Latch.4.4.pick	□ Latch.4.5	□ Latch.4.5.pick
□ Latch.4.6.guard	□ Latch.4.7	□ Latch.4.7.guard	□ Latch.4.10
□ Latch.5.1	□ Latch.5.3	□ Latch.5.4	□ Latch.5.5
□ Latch.5.6	□ Latch.4.8_Latch.4.9_Latch.5.2		
□ 5.2A_M3	□ 5.2B_M3	□ Off_Grid	□ SkewEdge
□ ANT.3.1.1D.ME*	□ ANT.3.1.2.NoTE2.VI*		

List of DRC-deviated errors on the memory generated by U18 Memory Generate.	
□ ANT.1D.b.ME1	The error can only occur in the memory generated by U18 Memory Generate.
□ ANT.1D.b.ME2	
□ ANT.1D.b.ME3	

UMC18 List of Other DRC-deviated Errors	
※ **Attention: If there are errors that TSRI does not allow, this case will not be allowed to tape out.**	
DRC error number	Causes of DRC errors

9-6 LVS verification

9.6.1 Are there LVS errors in this design case? □ Yes □ No

9.6.2 Is there a blackbox not provided by TSRI? □ Yes □No

9.6.3 Name of verification LVS software used: □ Calibre LVS □ _____

9.6.4 The LVS verification file name uploaded to the tape-out electronic webpage: _____

9.6.5 Does the file uploaded to the electronic tape-out webpage match the information filled out above? □ Yes □ No

9.6.6 Please verify the DRC verification result file on the queue server, especially the lvs.rep.ext file content in the Short_Check_With_Dummy data, to see if a lvs.rep.short file appears, or if there are any other LVS errors or warning messages relating to signal short circuits: □ Yes □ No

Notes: Through the online post-layout transistor level simulation on the queue server, the designer can self-verify whether the error occurrence affects the circuit design function.

10. Is the memory generated by the memory generator used? ■ Yes □ No

10-1 The cell name of the memory used: ***SRAM_2048x16***

10-2 Has memory used been approved by DRC inspection: ■ Yes □ No

11. Design synthesis

11-1 Synthetic software used: ***Synopsys Design Compiler***

11-2 Is the boundary condition added? ■ Yes □ No

■ input drive strength ■ input delay ■ output loading ■ output delay

11-3 Is the timing constraint added? ■ Yes □ No

■ specify clock (sequential design)

□ max delay □ min delay (combinational design)

11-4 Is there a timing violation in the synthesized report?

□ There is setup time violation. □ There is hold time violation.

11-5 Is there an assignment description in the synthesized verilog? □ Yes ■ No

11-6 Is there the instance name of *cell* in the synthesized verilog? □ Yes ■ No

12. Testability design (If a testability design is not used, check “No” and 12.1.1 ~ 12.1.5 need not be filled out.)

12-1 Is a testability design used? ■ Yes □ No

12.1.1 Design software used: **Synopsys DFT Compiler**

12.1.2 ATPG software used: **Synopsys TetraMax**

12.1.3 Quantity of embedded memory used: SRAM ***1*** , ROM ***1***

Memory size: **SRAM: 512 X 8, ROM: 128 X 8**

Test method: IST ***YES***, or other test methods _____

What is the test algorithm if BIST is used? **March C-**

There are multiple memories at the same time. Is the BIST controller used? ■ Yes □ NO

Quantity of BIST controllers: ***2***

12.1.4 Scan Chain Information

How many flip-flops are there? ***495***

How many scan chains are there? ***8***

Scan chain length (Max.): ***650***

12.1.5 Does the uncollapsed fault coverage exceed 90%? ■ Yes □ No, it is: ***95.67%***

How many ATPG patterns are there? ***348***

Note: If Synopsys TetraMA is used to generate the ATPG pattern, please use the set faults -fault_coverage command, designate TetraMAX to generate fault coverage information.

Use the atpg pessimistic fault coverage as the basis if asicgen of SynTest TurboScan is used to generate the ATPG pattern.

13. Pre-layout simulation

13-1 Does the gate level simulation have setup timing violation? □ Yes ■ No

14. Physical layout

14-1 P&R software used: □ IC Compiler ■ Innovus

14-2 Power ring width: ***40*** μm Is the current density considered: ■ Yes □ No

14-3 Quantity of IO power pads: ***5***; quantity of core power pads: ***5***

14-4 Quantity of IO ground pads: ***5***; quanity of ground pads: ***5***

14-5 Is the output loading considered? ■ Yes □ No

14-6 Is the clock tree added? ■ Yes □ No

Below (C-1) only need to be filled out by IC Compiler users.

C-1. : Is the route verification step executed and the violation corrected? ■ Yes □ No

Below (S-1 to S-2) only need to be filled out by Innovus users.

S-1. Is the connectivity verification step executed and error-free connectivity confirmed? ■ Yes □ No

S-2. Is the geometry verification step executed and the geometry violation corrected? ■ Yes □ No

15. Post-layout simulation

15-1 Has the post-layout gate level simulation been handled? ■ Yes □ No

STA (static timing analysis) software: **PrimeTime**

15-2 Has post-layout transistor level simulation been handled after replacing the queue server? ■ Yes □ No

(It is recommended that the post-layout transistor level simulation be completed if the ADPLL IP provided by CIC is used.**)**

15-3 The following environment statuses have been simulated: ■ SS ■ TT ■ FF

15-4 Which testing method is used during chip acquisition? **CIC 93000 test machine**

15-5 Are output load effects taken into account during APR? ■ Yes □ No. If there is an output load, it is as follows: ***40*** pF

16. Andes N1213-30T2G CPU IP is used.

16-1 If Andes N1213-30T2G CPU IP is used, please provide the following information:

The cell name of Andes N1213-30T2G Macro cell during layout: _____

Has the Consent Form for Authorization Fee for SRAM Use been signed and submitted? _____

Is this chip a revision, or is it identical to those that were previously taped out? _____

If it is a revised version, the next tape-out chip number is: _____

Reason for revising the version (such as correcting bugs): _____

17. Wire bonding diagram

17-1 For the chip layout in the wire bonding diagram, please use Virtuoso or Laker, and layouts opened using other layout editors to wire label. Do not use layouts opened using Innovus or IC Compiler, and other APR

tools. Has it been verified? ■ Yes □ No

17-2 To enable the packaging manufacturer to execute wire bonding operations according to the actual location of the layout IO pad wire bonding thread, the reference location must be labeled in the bottom left corner of the chip on the layout plan and wire bonding diagram. Has it been verified? ■ Yes □ No

Signature of designer: _____ Signature of advisor: _____

(Please ensure that this document is fully completed and submit the electronic file. No physical copy is required for submission.)