Confidentiality level: For internal use

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Tape-out Review Form *(for Full-custom IC)*

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The Tape-out Review Form is intended to remind designers to demonstrate design concepts and comprehend design, simulation, layout verification, and tape-out notes. It is hoped that the success rate of IC design and comprehensive learning results can be improved. As a result, the adviser and designer are asked to double-check that the requirements in this form were noted during the chip design process. If the design content and completion of the Tape-out Review Form are found to be inconsistent during review, the chip tape-out manufacturing qualifications will most likely be canceled.

Project name: Example of TSRI Tape-out Review Form

Name of Top Cell: TSRI EXEMPLE

Process name: T18

1 Circuit overview:

1-1. Work voltage: 3.3V

1-2. Work frequency: 20MHz

1-3. Power consumption: 3mW

1-4. Is ARM CPU IP provided by TSRI used? No

What type of CPU is used? (ARM7TDMI or ARM926EJ) ____

1-5. Is this the initial circuit architecture that your laboratory has designed? Yes (proceed to 2-1) No (proceed to 1-5-1) ____

1-5-1. What are the causes of previous subpar circuit measurement work or performance? ____

1-5-2. What changes have been made to previous errors? ____

2 Circuit simulation considerations

2-1. Which spice model simulation statuses have been used in SS, SF, TT, FS, and FF? Each of the five corners has been simulated.

2-2. Have the scenarios that affect circuit work when voltage changes are +/-10% been simulated? 2.97V~3.63V complies with the design.

2-3. In what manner are variations in temperature accounted for in their effects? Initiate simulation with temperatures ranging from 0 to 100 degrees.

2-4. In what manner are process variations in capacitance and resistance accounted for in their effects? The maximum and minimum variation values should be substituted into the simulation.

2-5. During simulation, are the effects of the IO PAD and bonding wire included, as well as taking into account the test instrument load and other effects? Yes

2-6. Are LPE and post layout simulation performed? Yes Software used: Calibre &

HSPICE

3 Power Line layout considerations

3-1. What is the width of the power line? 20um

3-2. Is power line current density taken into account? Yes

3-3. Are the parasitic resistance and capacitance of the metal line taken into account? Yes

4 DRC, LVS

4-1. Is it confirmed that the most recent versions of the DRC and LVS Command Files are in use? Yes

4-2. Are the DRC and LVS of whole chips performed? Yes

4-3. Have flat DRC and hierarchical DRC been verified during DRC verification? Yes

4-4. Is the density rule taken into account? Yes Is the filling method manual dummy cell filling of dummy generation filling? manual dummy cell filling until the density rules are complied.

4-5. Are there any errors in the internal circuit or pad connection wiring aside from the DRC error on the pad? No

What are the causes of errors? ______

4-6. During the LVS process, does the pin and component match? Yes What is the reason for the mismatch? ______

______

4-7. Verify whether a short circuit, displacement, or broken circuit is present between the pads. Yes

4-8. Verify whether the area of the bare pad is disproportionately small, whether windows are ajar, and whether there are any measurement considerations. Yes

5 ESD I/O PAD considerations

5-1. Create instance is the approach used to add I/O Pad, and copy or flatten destruction of instance structure are not used. Yes

5-2. In the IC core, wiring from pad only extends to the outermost edge, not excessively covering Pad. Yes

5-3. Is TSMC I/O PAD used (D35 process fill-out)? Yes

5-3-1. The personalized design cell name is not the same as any of the pad cell names provided by TSMC. Please make a thorough check. It has been verified.

6 Analog-Mixed signal circuit layout considerations (analog-filled out by the mixed signal circuit designer)

6-1. Layout symmetry and consistency considerations

6-1-1. Is the OP (comparator) input stage symmetrical? Yes

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6-1-2. Is the dummy cell technique used in symmetrical components during layout? Yes

6-1-3. Is a concentric circle layout used for symmetrical capacitors? Yes

6-1-4. Does the symmetrical unit capacitor have 45-degree angles cut on its edges? Yes

6-1-5. Is the unit area of the symmetrical capacitor consistent? Yes

What is the size of the area of the unit capacitor? 33 um x 33 um

What is the size of the unit capacitance value? 1 pF

Are the upper and lower bipolar plates connected correctly? Yes

6-1-6. What material is a resistor made of? Poly2

What is the size of the unit resistance value? 50Ω

6-2. Circuit noise layout considerations (filled out by the mixed signal circuit designer).

6-2-1. Will the power lines of analog and digital be separated? Yes

6-2-2. Is a guard ring being used to isolate the analog area? Yes

6-2-3. Is a guard ring used to isolate the digital area? Yes

6-2-4. Is the shield technique used for the sensitive line? Yes

6-2-5. Are the analog guard ring and shield connected to a clean potential? Yes

6-2-6. Is the sensitive line shortened as much as possible to avoid crossing the noise (clock) line? Yes

7 MEMS design considerations (filled out by the MEMs designer)

7-1. Please briefly describe post-processes undertaken: First, engage in etching and then incorporate carbon nanotubes.

7-2. Location of post-process operations: Asia Pacific Microsystems, Inc.

7-3. Is the person performing the tape-out task legally authorized to operate the process equipment? Yes If there is currently no legal authorization to operate the process equipment, can legal authorization be obtained before retrieving the chips? Yes

7-4. Is the individual performing the tape-out task experienced in operating the process equipment? Yes

7-5. Are post-process parameters available (pressure, temperature, flow, etc.)? Yes

7-6. Has the post-process previously been implemented successfully? Yes

7-7. Will the layout part that violated the design rule have an effect on the microstructure or component operations? No

7-8. Is the size of the etching hole adequate to suspend structures? Yes

7-9. What is the range of the component drive voltage? 0~3.3V

8 RF Circuit layout considerations (filled out by the RF operation frequency designer):

8-1. Which system meets the requirements of the circuit specification? 802.11b/g

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8-2. Explain the source of the passive component model. ____Obtained from EM simulation.____

8-3. Simulation software (more than one type is possible) ____ADS Circuit____

8-4. Have the respective blocks of system-integrated chips undergone tape-out and met the expected specifications (the chip is the system integrator answer and the process MPW run code)? _____

8-5. Layout considerations:

8-5-1. Is the component layout method consistent with the layout provided by the model provider? ____Yes____

8-5-2. Are ground and voltage sources uniform? ____Yes____

8-5-3. Are current carrying capacities of components and wiring factors to be considered? Yes____

8-5-4. Is the wiring excessively long and thin? ____No____

8-5-5. Does the PAD layout take measurement considerations into account? ____Yes____

8-5-6. Are the pad and bond wire effects taken into account? ____Yes____

8-6. Please specify if some of the errors are special considerations during the DRC verification process.____

____The CTM.R2 density is inadequate, which is listed as an allowable error in accordance with TSRI regulations.____

8-7. Has the comparison of inductors, capacitors, or other special components been handled during the LVS verification process? Please elaborate.____

____There is a self-made inductor on the circuit, and the short-circuit inductor undergoes an LVS comparison. After comparison, no error was found.____

8-8. Is the measurement method on wafer, on PCB or in package? Also explain notes during measurement and the measurement location.

____For the measurement of On Wafer, the measurement location is a laboratory with a high CIC frequency.____

9 GIPD circuit layout consideration (filled out by the GIPD, GIPD/T18 designer):

9-1. The issue of non-flat GIPD processes is likely to result in insertion measurement failure. (Please consult Attachment A for the environment and layout document pertaining to GIPD processes.) The design of the insertion pad has incorporated a higher degree of flatness in the insertion area to facilitate insertion measurements. Has it been verified? The pad has been thoroughly checked, and the explanation document has been thoroughly read.____

9-2. The following is filled out by the GIPD/T18 designer:

9-2-1. Have 1. the overall layout file (including the T18, bumper, and GIPD layers) and 2. the T18+bumper layout file been submitted for the layout? Furthermore, an independent mirror flip is absent. Has it been verified?____Yes____

9-2-2. The Bumper layout file is provided by CIC and is modified independently modified or innovative bumper layout. Has it been verified?____Yes____

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9-2-3. The quantity of bumpers is inadequate to support the T18 chip load. The exact number of bumpers required to correspond with the length has been carefully computed. Has it been verified? Yes

9-2-4. The T18 area must be greater than 1mm*1mm for CIPD/T18 integration chips, and the insertion pad distance from the T18 chips must be a minimum of 400um. Has it been verified? Yes

9-2-5. Top Metal is used to create GIPD/T18 integration chips and layout files that meet the fiducial mark required for flip chip packaging per DRC specifications. Furthermore, the layout plan includes detailed markings. Has it been verified? Yes

10 HV circuit design consideration (filled out by the T18HVG2/T25HVG2 designer):

10-1. Have the three DRC verifications been approved?

- ■ Wire-bond Rule ■ Main Design Rule ■ Antenna Rule

10-2. The OD/PO/Metal Density rule has been approved.

- ■ Yes □No (Application cases will not be accepted if the density is not complaint with the specifications.)

10-3. (0,0) are the coordinates of the whole chip's lower left corner.

- ■ Yes □No

10-4. Select the whole chip using the ref (drawing) (0;0) layer.

- ■ Yes □No

10-5. Are high-voltage transistors, BJTs, diodes, resistors and other components utilized in the circuit?

- □ No
- ■ High voltage transistors: ____
- □ BJT: ____
- ■ Diodes: ____
- ■ Resistance: ____
- □ Others: ____

10-6. Is there a protective circuit design?

- □ No ■ over-voltage protection ■ over-current protection ■ over-temperature protection ■ ESD protection circuit
- □ Other protections and considerations: ____

10-7. What is the circuit type?

- ■ High-voltage component structures and characteristics ■ power conversion circuit ■ LED drive ■ detection and protection ■ topology control ■ energy extraction □ biomedical applications □ others: ____

11 T50GaN circuit design considerations (filled out by the T50GaN designer):

11-1. Have the following DRC verifications been approved?

- ■ Main Design Rule

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11-2. (0,0) are the coordinates of the whole chip's lower left corner.

■ Yes □No

11-3. Components used in the circuit:

□ No

■ Components used: ______________________________

____

11-4. Is there a protective circuit design?

□ No ■ over-voltage protection ■ over-current protection ■ over-temperature protection ■ ESD protection circuit

□ Other protections and considerations: ______________

11-5. What is the circuit type?

■ High-voltage component structures and characteristics ■ power conversion circuit ■ high-speed drive circuit ■ EV related applications ■ high-power wireless charging ■ radar and laser related applications □ others: ______________

12 U18 circuit design considerations (filled out by U18 designers)

12-1. Have the following DRC verifications been approved?

■ Base Rule ■ ANT Rule ■ DIFF Rule ■ ESD Rule ■ Latch-up Rule

■ Metal Rule ■ OPC Rule ■ PAD Rule ■ POLY Rule

12-2. In the CMOS layout, has the DMBK Layer been selected?

■ PO_CAD(DK) ■ DIFF_CAD(DK) ■ M1_CAD(DK) ■ M2_CAD(DK) ■ M3_CAD(DK) ■ M4_CAD(DK) ■ M5_CAD(DK) ■ M6_CAD(DK)

12-3. In the MEMS layout, in addition to the above-mentioned 12-2 DMBK Layer, has the M7 DMBK Layer been selected?

■ M7_CAD(DK)

12-4. The illustrated nine test results of the DRC Rule should be enumerated and explained individually in the design content e-file. Additionally, consult the page for the Design Rules Check (DRC).

■ It has been verified.

12-5. If it is necessary to deviate design requirements from the DRC, please fill out the Application Form for Deviation from DRC to the U18 process engineers through email as soon as the DRC verification results are available.

■ It has been verified.

12-6. For the Dummy Layer, it is advisable to utilize PO_CAD(Dy), DIFF_CAD(Dy), M1_CAD(Dy), M2_CAD(Dy), M3_CAD(Dy), M4_CAD(Dy), M5_CAD(Dy), M6_CAD(Dy), and M7_CAD(Dy) instead of the DMBK Layer.

■ It has been verified.

13 ARM926EJ or ARM7TDMI CPU IP is used.

13-1. If ARM926EJ /ARM7TDMI CPU IP are used, please provide the information below to submit

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a Design ID application to the ARM manufacturer.

CPU type used (ARM926EJ or ARM7TDMI): ARM926E

The number of metal layers used: 6

The cell name of ARM926EJ /ARM7TDMI Macro during layout: TEST

Is this chip a revision, or is it identical to those that were previously taped out? No

If it is a revised version, the next tape-out chip number is: ____________

Reason for revising the version: (such as bug correction) ____________

14 Other considerations

14-1. Is the output measurement point during testing taken into account? Yes

14-2. Is the modifiability of circuits taken into account? (such as laser cut equipment) Yes

Signature of designer: Wang Hsiao-Ming   Name of advisor: Li Ta-Ming

(Please ensure that this document is fully completed and submit the electronic file. No physical copy is required for submission.)

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