PCB Fabrication Design Rule Manual

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PCB Problem?
Client Service System
www.tsri.org.tw

Versions

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Contents

1. Preface 1

2. PCB Process Introduction 2

2.1 FR4 2-Layer Board.. 3
2.2 FR4 4- layer Board 5
2.3 RO4003C High-Frequency 2-Layer Board 7
2.4 RO-FR4 Complex 4-layer board 9
2.5 PCB layer Naming 11

3. Material Parameters 12

3.1 Dielectric 12
3.2 Metal 14

4. PCB layout design rule 16

4.1 Design rule naming, summary and FAQ 16

4.1.1 Design rule naming 16

4.1.2 Design rule summary 17

4.1.3 Design rule FAQ 20

4.2 Metal 21

4.2.1 Metal line design rule 21

4.2.2 Copper design rule... 22

4.3. Drill and Ring 23

4.3.1 PTH and ring design rule 24

4.3.2 Non-Plated Through Hole (NPTH) design rule 26

4.3.3 Slot (PTH and NPTH) design rule 27

4.4 Solder Mask layer 28

4.4.1 Solder Mask layer design rule 28

4.4.2 Solder Mask layer Notice 30

4.5 silkscreen 32

4.5.1 Silkscreen design rule 32

4.5.2 “PCB Identification Code” Marking 34

4.6 Mechanical layer 35

4.6.1 PCB fabrication size, shape and billing 35

4.6.2 Board Outline BO frame and Position Hole NH design rule 37

4.6.3 PCB cut out design rule 39

4.6.4 ME Frame 40

4.6.4.1 ME frame design rule 40

5. Chinese and English noun contrast 42

6. References 43

1. Preface

This manual is provided by TSRI to design PCB FR4 2-Layer Board, FR4 4-layer board, RO4003Chigh frequency 2-Layer Board and RO4003C-FR4 complex 4-layer board data. The data includes PCB stackup (Stacking), material parameters, and layout design rules.

2. PCB Process Introduction

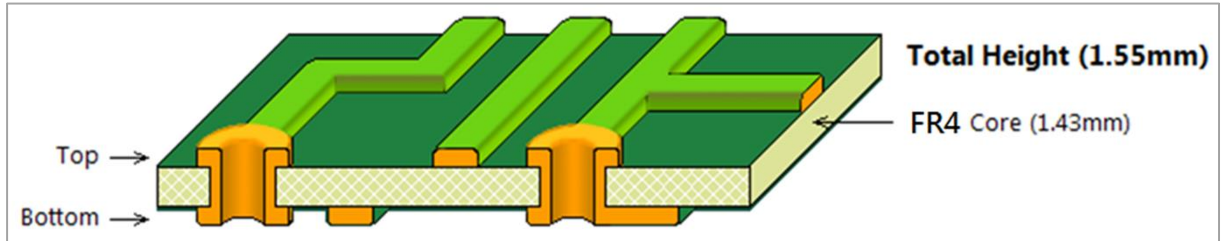
Terminology introduction:

process	**Remarks**
Copper	External and internal metal layers use copper (Cu) material. The thickness is 1 oz (0.034 mm) or 1/2 oz (0.017 mm). It is used for connection, power layer, etc.
PTH	Plating Through Hole, hole side wall is plated with copper. Conducting electric current. PTH is used to connect 2 or more than 2 metal layers, the pad of DIP components, or connect to (metal) enclosures, etc...
NPTH	Non-Plating Through Hole Hole side-wall is NOT plated with copper. Conducting electric current. NPTH is simply mechanical drill. Used for assembly.
Solder Pad	Exposed copper metal without solder Mask. Usually for soldering use. Surface treatment with ENIG. See figure below, yellow color Ni/Au) to prevent copper oxidation. Used as SMD or DIP component pins, bonding pad, or test points.
Solder Mask layer	Double sides Protect pads being short-circuited when soldering.
Silkscreen	Double sides Markings for components, net traces, or test points.
Mechanical layer	Mechanical process use. Used for PCB Board Outline and ME Frame.

Table 2-1 PCB process terminology

2.1 FR4 2-Layer Board

Stackup:



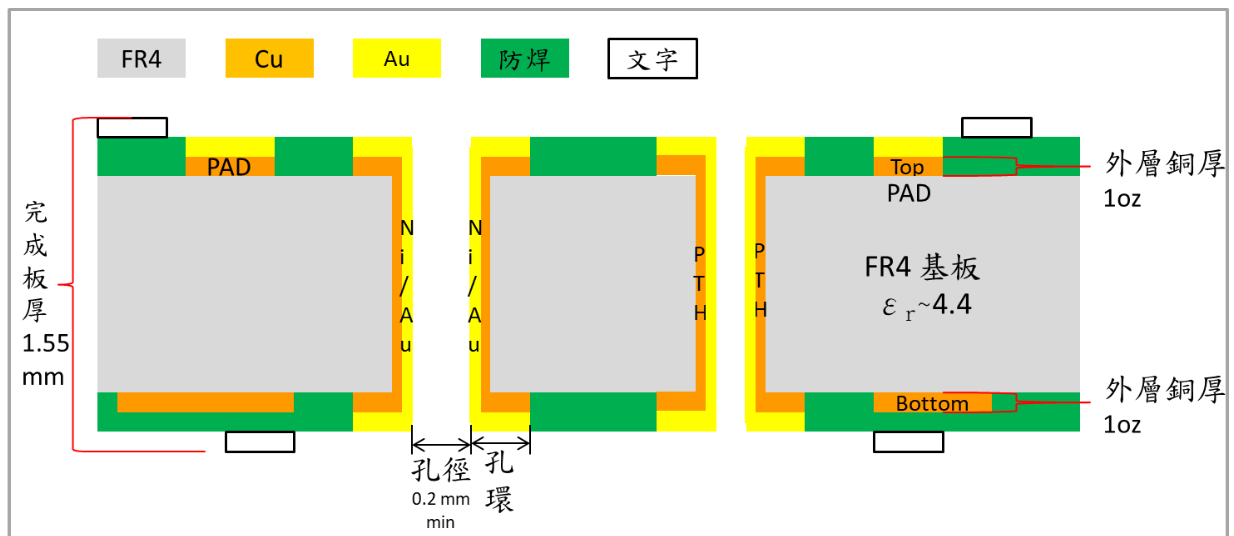


Fig. 2.1-1 FR4 2-Layer Board stackup Figure (3-D Figure and side Figure)

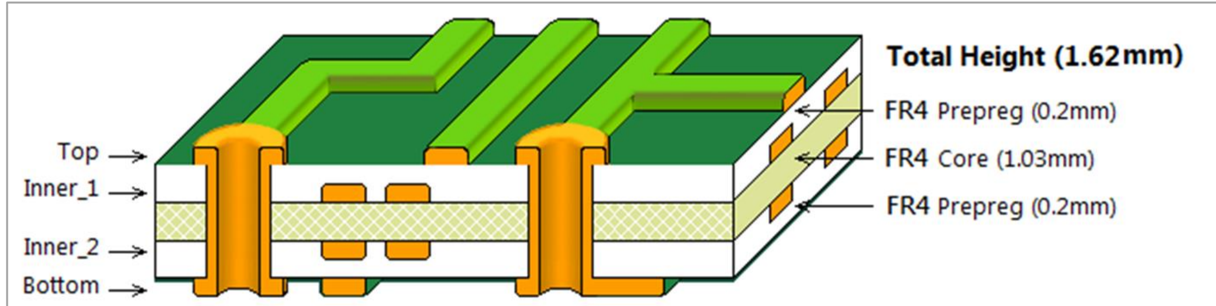
Thickness:

Item	Value (Unit mm)	Remarks
silkscreen thickness	0.017	
solder Mask thickness	0.025	
copper thickness _Top	0.035	1 oz
FR4 substrate thickness	1.430	
copper thickness _Bottom layer	0.035	1 oz
solder Mask layer thickness	0.025	
silkscreen thickness	0.017	
Finished Board thickness	1.550	Not including silkscreen layer thickness
Finished Board thickness _tolerance	10%	

Table 2.1-1 FR4 2-Layer Board stackup thickness data

2.2 FR4 4- layer Board

Stackup:



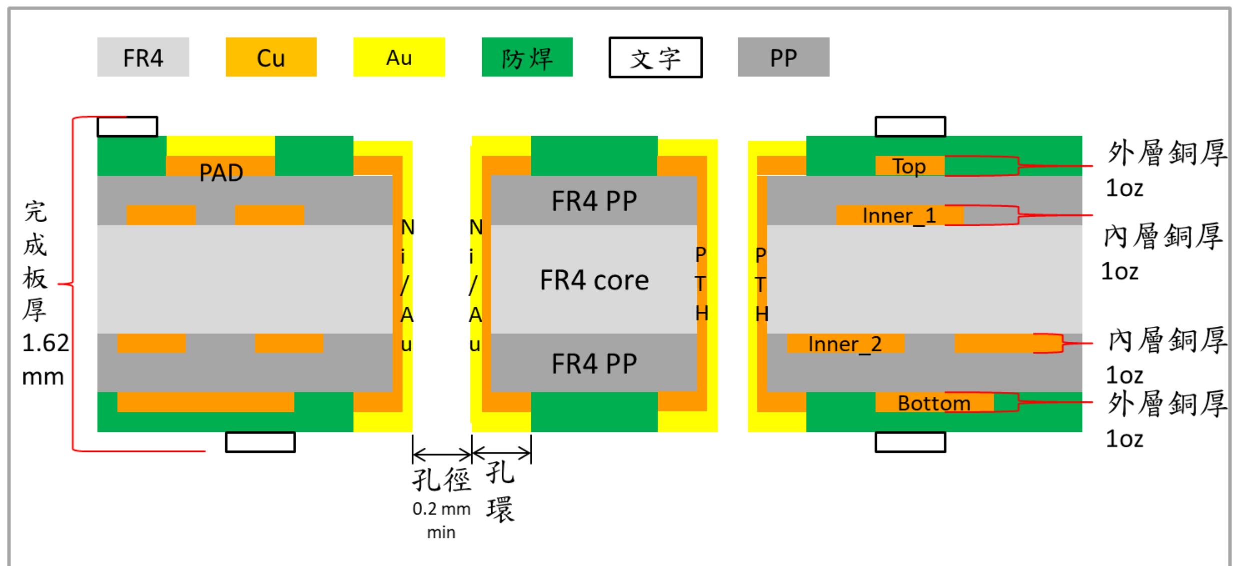


Fig. 2.2-1 FR4 4-layer board stackup figure (3D figure and side figure)

Thickness data Table:

Item	數值 (Unit mm)	Remarks
silkscreen thickness	0.017	
solder Mask layer thickness	0.025	
copper thickness _Top layer	0.035	1 oz
FR4 PP layer thickness	0.200	
copper thickness _Inner_1 layer	0.035	1 oz
FR4 substrate thickness	1.030	
copper thickness _Inner_2 layer	0.035	1 oz
FR4 PP layer thickness	0.200	
copper thickness _Bottom layer	0.035	1 oz
solder Mask layer thickness	0.025	
silkscreen thickness	0.017	
Finished board thickness	1.620	Not including silkscreen thickness
Finished board thickness _ tolerance	10%	

Table 2.2-1 FR4 4-layer board stackup thickness data

2.3 RO4003C High-Frequency 2-Layer Board

Stackup:

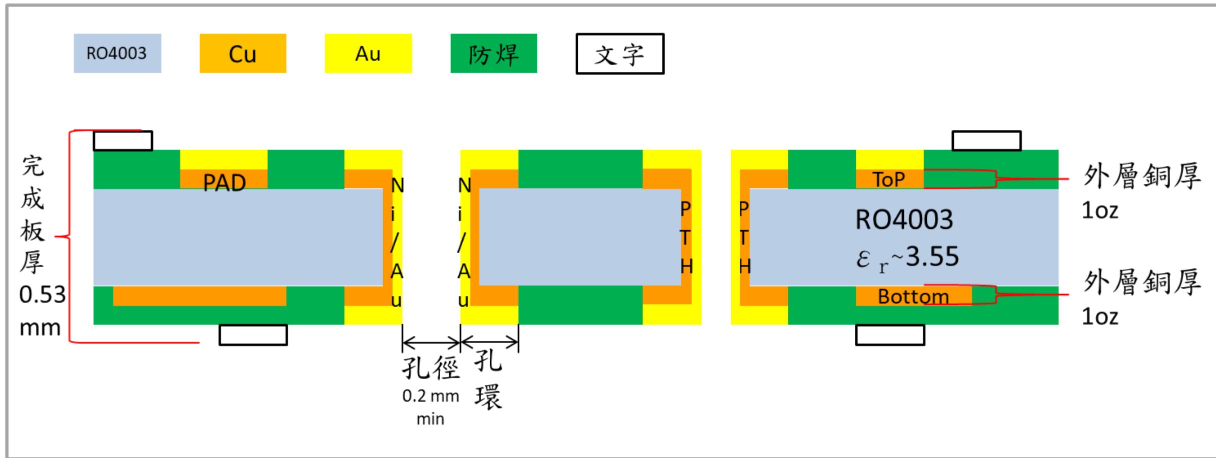


Fig. 2.3.2-1 PCB_2LHF16 process RO4003C 16mil 2-Layer Board stackup (3D figure and side figure)

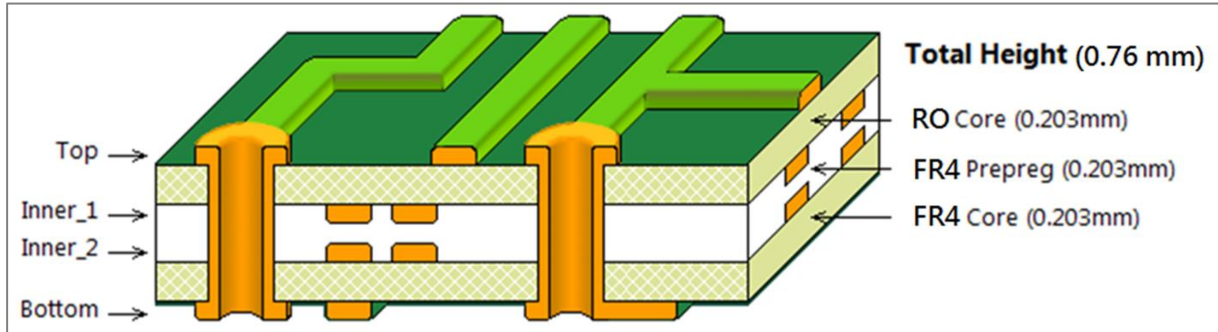
Thickness Table:

Item	Value (unit: mm)	Remarks
silkscreen thickness	0.017	
solder Mask layer thickness	0.025	
copper thickness _Top layer	0.035	1 oz
RO substrate thickness	0.406	16 mil
copper thickness _Bottom layer	0.035	1 oz
solder Mask layer thickness	0.025	
silkscreen thickness	0.017	
Finished board thickness	0.530	Not including silkscreen layer thickness
Finished board thickness _tolerance	10%	

Table 2.3.2-1 RO4003C 2-Layer Board stackup thickness data

2.4 RO-FR4 Complex 4-layer board

Stackup:



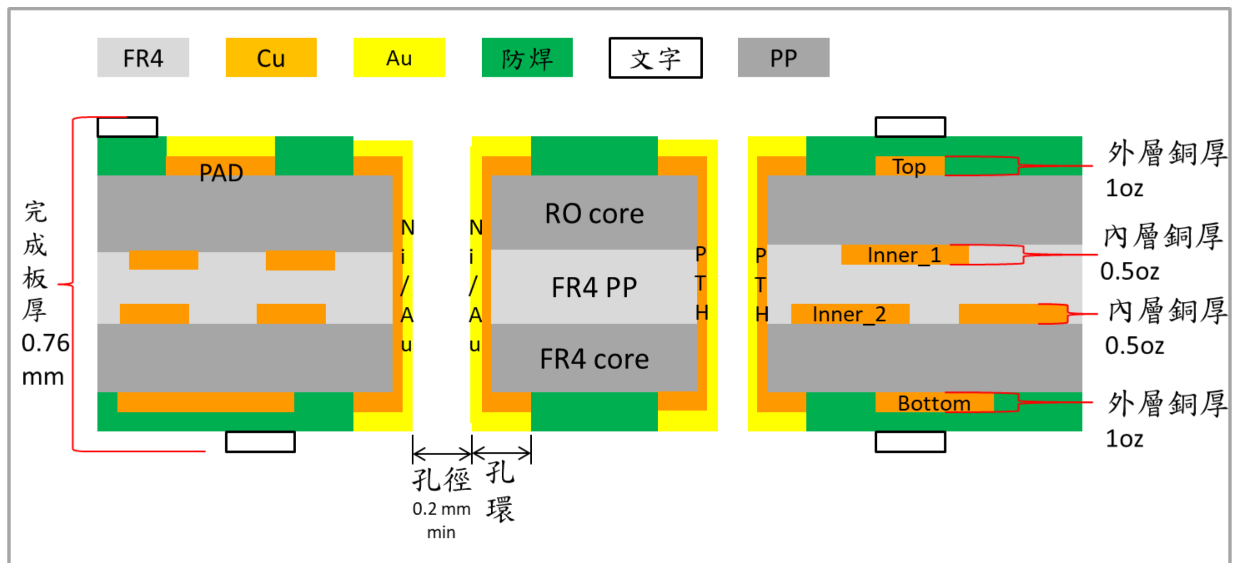


Fig. 2.4-1 RO-FR4 Complex 4-layer board stackup Figure (3D figure and side figure)

Thickness data Table:

Item	Value (unit mm)	Remarks
silkscreen thickness	0.017	
solder Mask layer thickness	0.025	
copper thickness _Top layer	0.035	1 oz
RO core thickness	0.203	8 mil
copper thickness _Inner_1 layer	0.017	½ oz
FR4 PP thickness	0.203	
copper thickness _Inner_2 layer	0.017	½ oz
FR4 core thickness	0.203	
copper thickness _Bottom layer	0.035	1 oz
solder Mask layer thickness	0.025	
silkscreen thickness	0.017	
Finished board thickness	0.763	Not including silkscreen layer thickness
Finished board thickness _tolerance	±0.1	

Table 2.4-1 RO-FR4 Complex 4-layer board stackup thickness data

2.5 PCB layer Naming

TSRI recommends the layer naming and DRC color as the following Table:

Recommend Name	Full Name	Layer Function	DRC Layer Name	DRC layer Color
TOP	Top	external metal layer Top	MT	
IN1	Inner_1 (4-layer board with)	internal metal layer L1		
IN2	Inner_2 (4-layer board with)	internal metal layer L2		
BOT	Bottom	external metal layer Bottom		
SMT	Solder_top	solder Mask layer _top	SO	
SMB	Solder_bottom	solder Mask layer _bottom		
SST	Silkscreen_top	silkscreen _top	SK	
SSB	Silkscreen _bottom	silkscreen _bottom		
NCD	NC Drill	drill layer	DR	
BO	Board Outline	Board Outline *	BO	
ME	Mechanical	ME Frame #	ME	

Table 2.5-1 PCB fabrication layer Naming and Color

* Board Outline : PCB actual shape

ME Frame: PCB fabrication size frame

3. Material Parameters

Most material parameters are provided by supplier. If the parameter is not provided by the supplier, there will be marks, such as @, * etc., and attach the value in Wi-Ki Encyclopedia. Designer can use these values at first try.

3.1 Dielectric

FR4 Dielectric:

material	FR4	FR4 PP	solder Mask layer
dielectric constant	4.4	4.4	3.63
dielectric constant _ tolerance	±10%	±10%	±10%
δ／Loss tangent@	0.017	0.017	0.0266
glass temperature (Tg*)	140℃	140℃	-
Tg_tolerance	+15%	+15%	-

Table 3.1-1 FR4 dielectric parameters

@ loss tangent: =DF (Dissipation factor),
http://en.wikipedia.org/wiki/Fr4 **,**
http://en.wikipedia.org/wiki/Dissipation_factor

***Tg**: glass transition temperature, or glass temperature < Tm (melting T)
(http://en.wikipedia.org/wiki/Glass_transition_temperature)

*RO-FR4 complex 4-layer board FR4 Tg=180℃

RO4003C dielectric #

material	RO4003C	RO4003C PP	solder Mask layer
dielectric constant	3.55	NA	3.63
dielectric constant _ tolerance	±0.05	NA	±10%
δ／Loss tangent @2.5GHz/23℃	0.0021	0.0021	0.0266
δ／Loss tangent @10GHz/23℃	0.0027	0.0027	-
glass temperature (Tg)	280℃	280℃	-
Tg_ tolerance	+15%	+15%	

Table 3.1-2 RO4003C dielectric layer parameters

 # RO4003C https://rogerscorp.com/en/advanced-connectivity-solutions/ro4000-series-laminates
https://rogerscorp.com/en/advanced-connectivity-solutions/ro4000-series-laminates/ro4003c-laminates

3.2 Metal

Metal Layer Properties
Metal layer range: external metal layer Top, internal metal layer IN1, IN2, and external Bottom copper layer.

Item	Unit	Remarks
材質	-	Cu
thickness	mm	0.035
Conductivity σ (at 20℃)#	$S \cdot m^{-1}$	$5.96x10^{7}$
Resistivity ρ (at 20℃)#	$\Omega \cdot m$	$1.68x10^{-8}$

Table 3.2-1 copper layer parameters
#:http://en.wikipedia.org/wiki/Electrical_resistivity_and_conductivity

PTH (Plating Through Hole) Properties

Item	Unit	Remarks
Material	-	Cu
thickness	mm	0.025
Conductivity σ (at 20℃) #	$S \cdot m^{-1}$	$5.96x10^{7}$
Resistivity ρ (at 20℃) #	$\Omega \cdot m$	$1.68x10^{-8}$

Table 3.2-2 PTH parameters
#:http://en.wikipedia.org/wiki/Electrical_resistivity_and_conductivity

Surface Treat ENIG

Item	Unit	Remarks
Material	-	Ni
Thickness	µm	3
Conductivity σ (at 20℃) #	S・m^{-1}	$1.43×10^{7}$
Resistivity ρ (at 20℃) #	Ω・m	$6.99×10^{-8}$

Table 3.2-3 Surface Treatment material Ni parameters

Item	Unit	Remarks
Material	-	Au
Thickness	µm	0.025~0.05
Conductivity σ (at 20℃) #	S · m^{-1}	$4.10×10^{7}$
Resistivity ρ (at 20℃) #	Ω · m	$2.44×10^{-8}$

Table 3.2-4 Surface Treatment material Au parameters

#:http://en.wikipedia.org/wiki/Electrical_resistivity_and_conductivity

4. PCB layout design rule

4.1 Design rule naming, summary and FAQ

4.1.1 Design rule naming

Rule:

L1.	**L2.**	**R.**	**N**
(A)	(B)	(C)	(D)

(A) L1 is original layer (Original Layer), and 2-letter naming.
(B) L2 is destination layer (Destination Layer (if any)), and 2-letter naming.
(C) R is layer and layer relationship, 1-letter naming. See following:

Code	English	Chinese
L	Length	長
W	Width	寬
S	Spacing	間距
E	Enclosure	外圍

Table 4.1.1-1 design rule layer and layer relationship

(D) N: rule no.

4.1.2 Design rule summary

M: Must / O: Optional

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
metal line	1	MT.W.1	MW	metal line width	≧	0.10	M
	2	MT.S.1	MS	metal line to line distance	≧	0.10	M
	3	MT.BO.E.1	MB	metal line and Board Outline distance	≧	0.30	M
copper	4	MT.S.2	MC	copper to metal distance (FR4)	≧	0.18	M
				copper to metal distance (RO)	≧	0.17	M
	5	MT.BO.E.1	CB	copper and Board Outline distance	≧	0.30	M
Plated Through Hole (PTH) and ring	6	DR.W.1	D1	PTH drill min size	≧	0.20	M
	7	DR.W.2	D1	PTH drill max size	≦	6.00	M
	8	DR.DR.S.1	D4	PTH drill to drill distance	≧	0.30	M
	9	DR.MT.S.1	D5	PTH drill to metal line distance	≧	0.30	M
	10	DR.BO.E.1	D6	PTH drill to Board Outline distance	≧	0.50	M
	11	MT.W.2	D2	PTH external metal layer ring line width	≧	0.10	M
	12	MT.SO.E.1	D3	PTH ring to solder Mask distance	≧	0.10	O
Non-Plated Through Hole (NPTH)	13	DR.W.3	N1	NPTH drill min size	≧	0.50	M
	14	DR.W.4	N1	NPTH drill max size	≦	6.00	M
	15	DR.DR.S.2	N2	NPTH drill to drill distance	≧	0.30	M
	16	DR.RU.S.2	N3	NPTH to Board Outline distance	≧	0.50	M

	17	DR.SO.E.2	N4	NPTH drill to solder Mask distance	≧	0.12	O
Slot (PTH and NPTH)	18	DR.W.5	O1	slot hole min size	≧	0.55	M
	19	DR.W.6	O1	slot hole max size	≦	6.00	M
	20	DR.DR.S.3	O2	slot hole center to center distance	≧	> O1	M
	21	DR.DR.S.4	O3	slot hole to distance	≧	0.50	M
	22	DR.RU.S.3	O4	slot hole to Board Outline distance	≧	0.80	M

Item	**No.**	**rule naming**	**Code**	**Remarks**	**calculating signs**	**size (mm)**	**rule feature M / O**
solder Mask layer	23	MT.SO.E.1	S1 =D3	metal PAD to solder Mask distance	≧	0.10	O
	24	SO.W.1	S2	solder Mask line width	≧	0.10	O
silkscreen	25	SK.W.1	SkW	Silkscreen line width	≧	0.15	O
	26	SK.H.1	SkH	Text height	≧	1.00	O
	27	SK.MT. S.1	SkM	silkscreen and PAD distance	≧	0.20	O
BO Layer	28	BO.W.1	BOW	Board Outline line width	=	0.10	M
	29	BO.H.1	NH	Position Hole diameter	≧	1.00	M
	30	BO.H.2	NH	Position Hole Feature	=	NPTH	M
	31	CO.R.1	COR	PCB cut out edge arc diameter	≧	1.00	M
	32	CO.W.1	COW	PCB cut out width	≧	0.80	M
	33	CO.L.1	COL	PCB cut out length	≧	0.80	M
	34	CO.M.E.1	COM	PCB cut out and metal distance	≧	0.30	M

	35	CO.B.E.1	COM	PCB cut out and Board Outline distance	≧	0.30	M
	36	CO.T.1	COT	Text in Cut Out	-	-	M
ME layer	37	ME.W.1	MEW	ME Frame line width	=	0.10	M
	38	ME.S.1	MES	ME Frame to Board Outline distance	=	1.50	M

Table 4.1.2-1 design rule summary

4.1.3 Design rule FAQ

Classification	Problem	Remarks	TSRI handling procedure
PAD	**Via on PAD**	Via on PAD design, which will might cause problems of reflow, the older will leak out through via, so that the firm soldering cannot be assured, and it might influence the bottom-side components. If the design is for thermal dissipation or grounding, it can be accepted for fabrication.	Ignore
Drill	drill without PAD	Violate DR.W.1 drill min size design rule. For different software, there might be warning, such as "zero hole size".	Ignore
solder Mask	Whole solder Mask layer no layout	Sometimes the designer forgets to plot any figures on solder Mask layer. The SM is negative plot, so there is no exposure of copper. This will cause solder failure.	Ignore
solder Mask	No PAD solder Mask layer No COB solder Mask layer	This will cause PAD and COB be painted by solder, and no copper exposure for soldering. COB: Chip On Board	Ignore
solder Mask	no solder Mask layer on via	This will cause via (especially for test points) be painted by solder, and no copper exposure for soldering.	Ignore
Metal	**layout plot with extra point, line or Figure**	Designer has to assign each Figure with net name.	Ignore
Other	**Need Paste layer Gerber file?**	No need for TSRI service.	Ignore

Table 4.1.3-1 design rule FAQ

4.2 Metal

4.2.1 Metal line design rule

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
metal line	1	MT.W.1	MW	metal line width	≧	0.10	M
	2	MT.S.1	MS	metal line to line distance	≧	0.10	M
	3	MT.BO.E.1	MB	metal line and Board Outline distance	≧	0.30	M

Table 4.2.1-1 metal line design rule

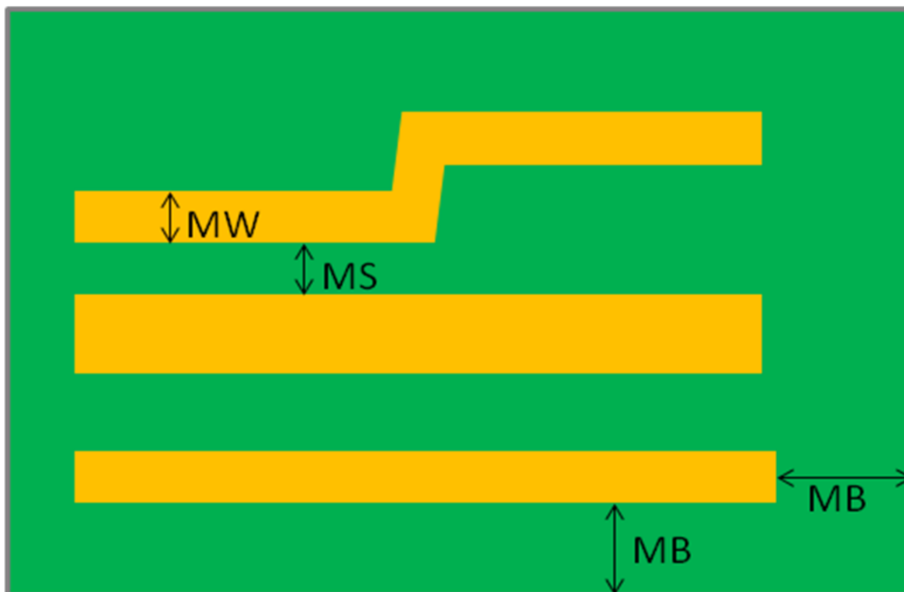


Fig. 4.2.1-1 metal line design rule

4.2.2 Copper design rule

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
copper	4	MT.S.2	MC	copper to metal distance (FR4)	≧	0.18	M
				copper to metal distance (RO)	≧	0.17	M
	5	MT.BO.E.1	CB	copper and Board Outline distance	≧	0.30	M

Table 4.2.2-1 copper design rule

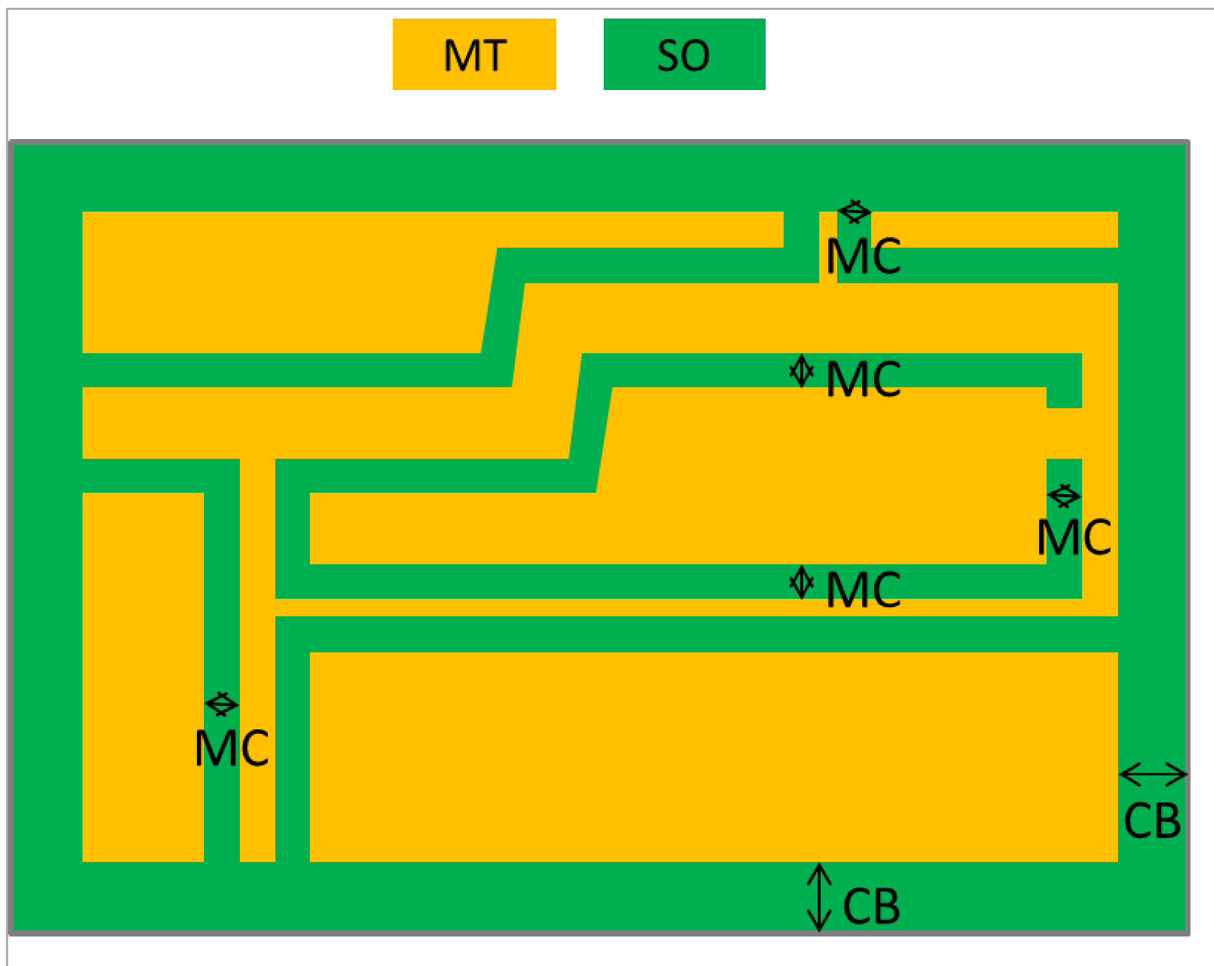


Fig. 4.2.2-1 copper design rule

4.3. Drill and Ring

Drill is Mechanical drill. After drilling, the inner part of drill will be plated or not plated with copper. TSRI provides through-hole process only, without partial hole, such as blind or buried holes. Through hole drill through the entire stackup, from Top to Bottom.

There are 2 kinds of drill holes: Plating through Hole (PTH), or non-Plating Through Hole (NPTH).

4.3.1 PTH and ring design rule

PTH drill-hole tolerance is ± 0.075 mm.

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
PTH and ring	6	DR.W.1	D1	PTH drill min size	≧	0.20	M
	7	DR.W.2	D1	PTH drill max size	≦	6.00	M
	8	DR.DR.S.1	D4	PTH drill to drill distance	≧	0.30	M
	9	DR.MT.S.1	D5	PTH drill to metal line distance	≧	0.30	M
	10	DR.BO.E.1	D6	PTH drill to Board Outline distance	≧	0.50	M
	11	MT.W.2	D2	PTH external metal layer ring line width	≧	0.10	M
	12	MT.SO.E.1	D3	PTH ring to solder Mask distance	≧	0.10	O
solder Mask layer	23	MT.SO.E.1	S1 =D3	metal PAD to solder Mask distance	≧	0.10	O
	24	SO.W.1	S2	solder Mask line width	≧	0.10	O

Table 4.3.1-1 PTH and ring design rule

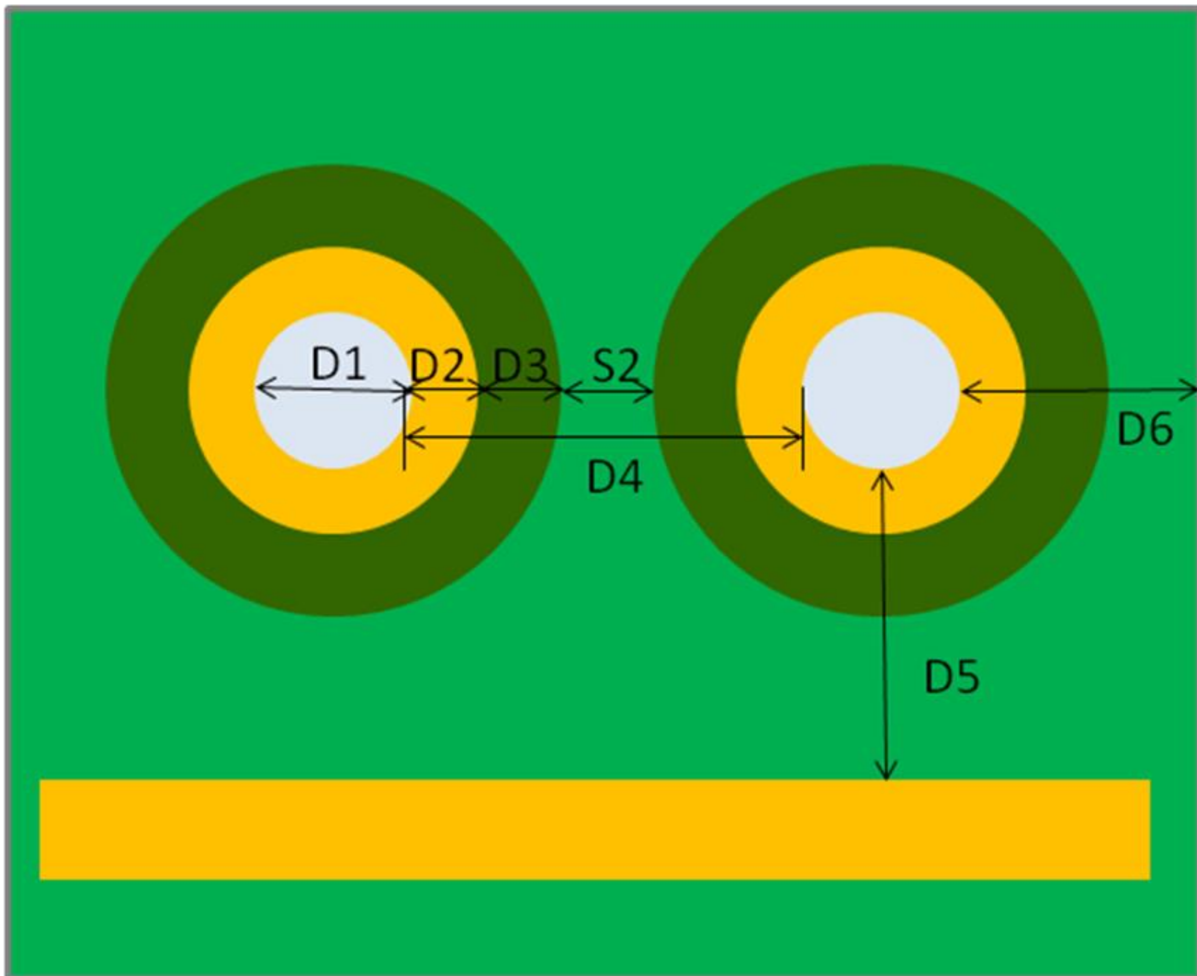


Fig. 4.3.1-1 PTH and ring design rule

4.3.2 Non-Plated Through Hole (NPTH) design rule

NPTH can be used as screw hole or auxiliary hole for fixing components. There is no copper plating inside hole. Tolerance is ± 0.075 mm. At the same time, NPTH should follow PTH design rule.

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
NPTH	13	DR.W.3	N1	NPTH drill min size	≧	0.50	M
	14	DR.W.4	N1	NPTH drill max size	≦	6.00	M
	15	DR.DR.S.2	N2	NPTH drill to drill distance	≧	0.30	M
	16	DR.RU.S.2	N3	NPTH to Board Outline distance	≧	0.50	M
	17	DR.SO.E.2	N4	NPTH drill to solder Mask distance	≧	0.12	O

Table 4.3.2-1 NPTH design rule

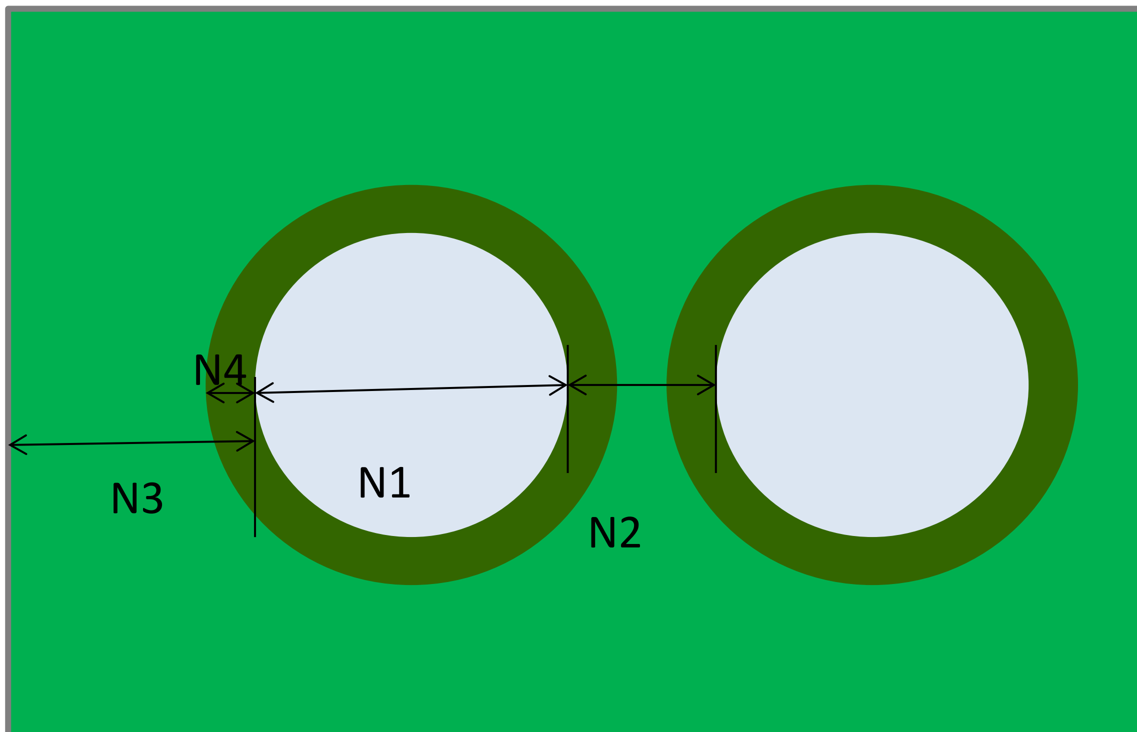


Fig. 4.3.2-1 NPTH design rule

4.3.3 Slot (PTH and NPTH) design rule

Slot can be used for DIP components, or screw holes, and can be plated or non-plated. tolerance± .At the same time, slot must follow PTH and NPTH design rule.

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
Slot (PTH and NPTH)	18	DR.W.5	O1	slot drill min size	≧	0.55	M
	19	DR.W.6	O1	slot drill max size	≦	6.00	M
	20	DR.DR.S.3	O2	slot drill to drill distance	≧	> O1	M
	21	DR.DR.S.4	O3	slot center to center distance	≧	0.50	M
	22	DR.RU.S.3	O4	slot to Board Outline distance	≧	0.80	M

Table 4.3.3-1 Slot design rule

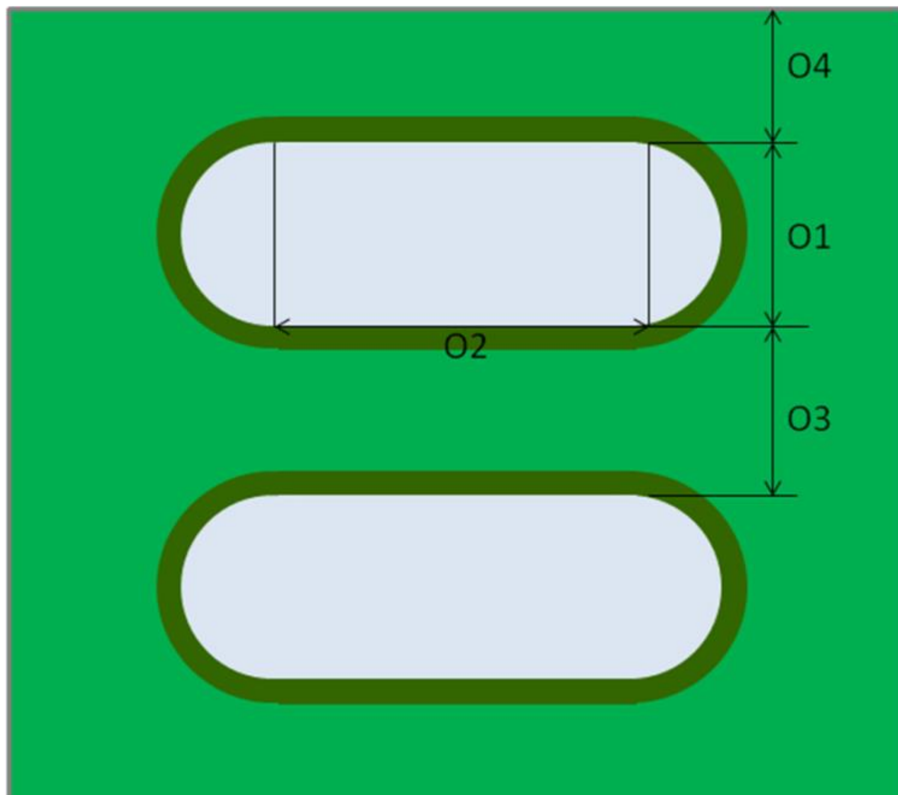


Fig. 4.3.3-1 Slot design rule

4.4 Solder Mask layer

4.4.1 Solder Mask layer design rule

Place to draw solder mask: PADs, test points, exposed copper metal.
Surface treatment: The exposed copper area will be surface treated by ENIG (Electroless Nickel Immersion Gold) to avoid oxidation.
Properties: Negative image.
Size: Usually solder Mask layer opening is larger than PAD.
Fail to fabricate: when distance of solder Mask to solder Mask is too small, such as Fig. 4.4.2-1 and Fig. 4.4.2-2 examples.

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
solder Mask layer	23	MT.SO.E.1	S1 =D3	metal PAD to solder Mask distance	≧	0.10	O
	24	SO.W.1	S2	solder Mask line width	≧	0.10	O

Table 4.4.1-1 solder Mask layer design rule

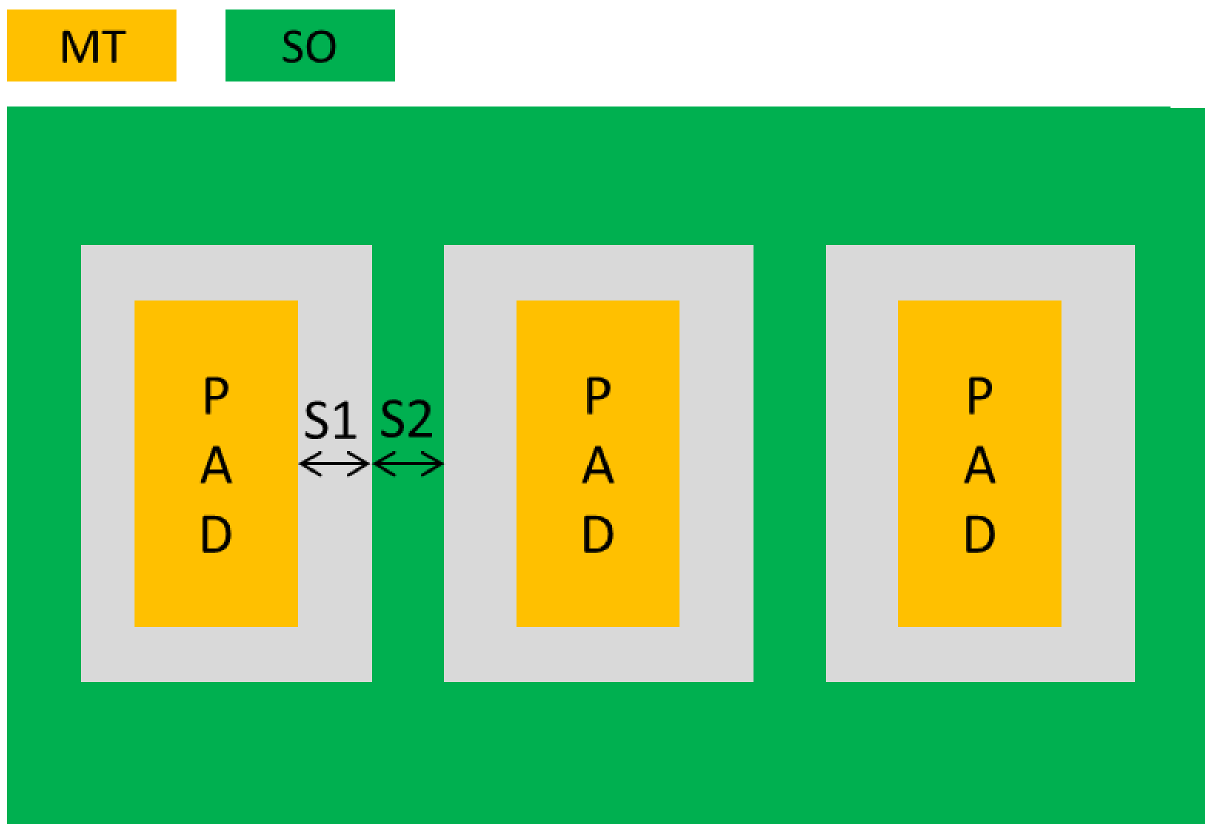


Fig. 4.4.1-1 solder Mask layer design rule

4.4.2 Solder Mask layer Notice

Solder Mask layer is negative.
Even window: when distance of solder Mask to solder Mask is too small, the solder will not be applied. When soldering, it is was easy to cause short-circuited.

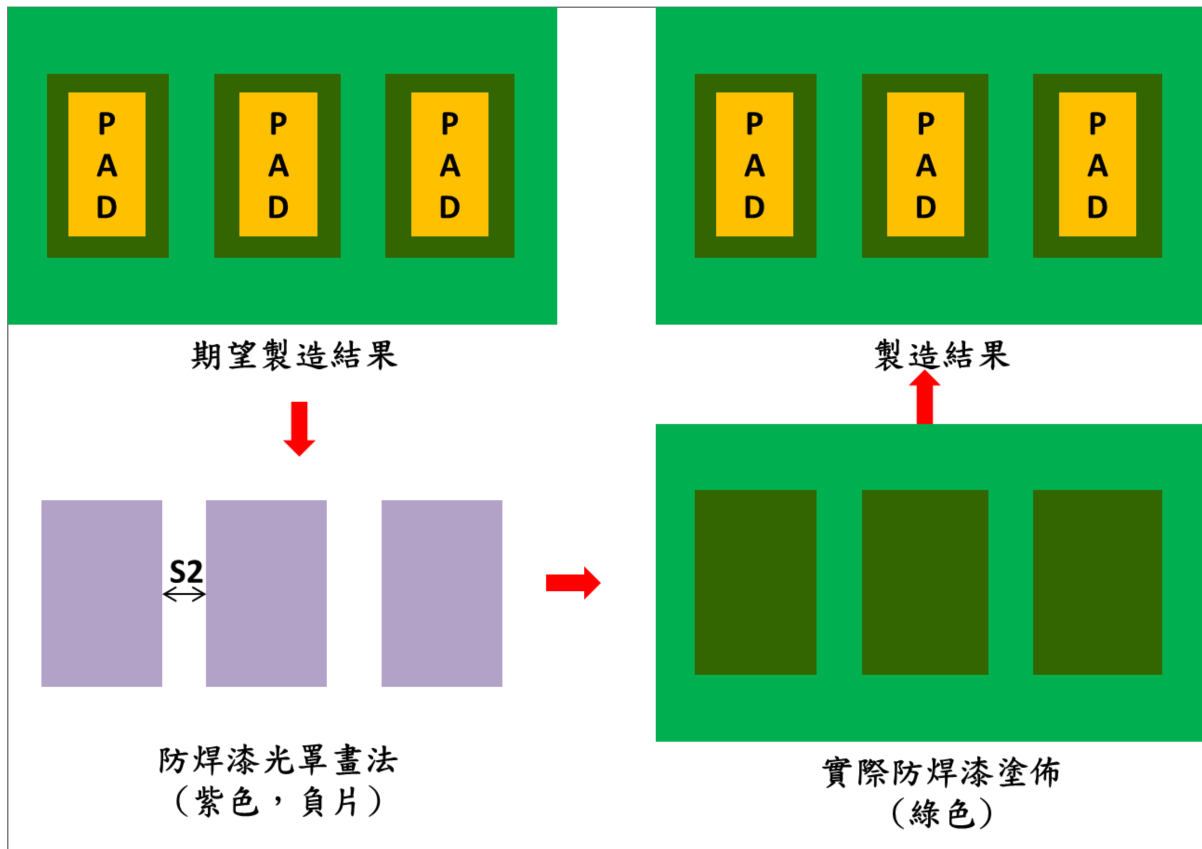


Fig. 4.4.2-1 “solder Mask min line width” S2 is enough

S2 is too small:

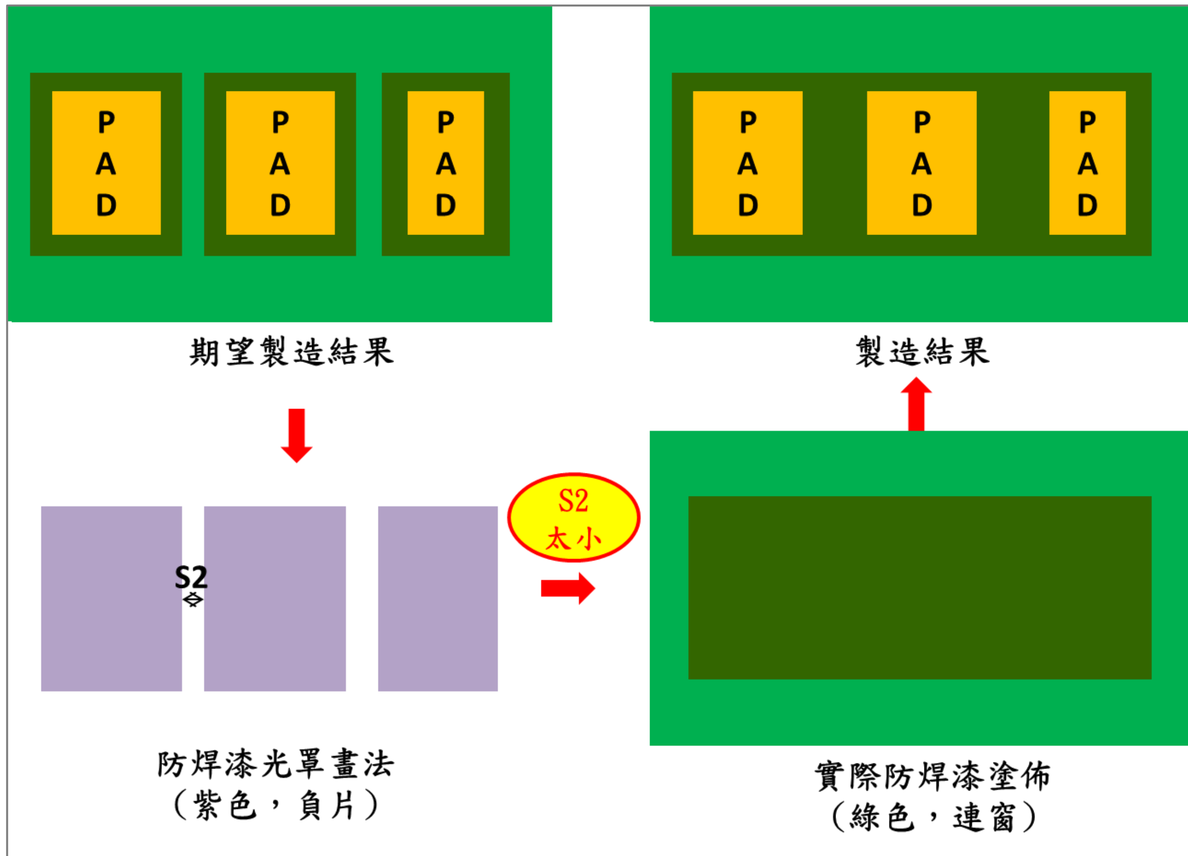


Fig. 4.4.2-2 “Solder Mask min line width” S2 is too small

4.5 silkscreen

4.5.1 Silkscreen design rule

Silkscreen layer is above solder Mask layer, usually it is used as marking for components, test points or traces, etc. The alignment tolerance within 0.25mm.

TSRI does not check silkscreen layer, so that the designer may not violate the rules. Otherwise, the texts might be blur, disappeared, etc.

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
silkscreen	25	SK.W.1	SkW	silkscreen line width	≧	0.15	O
	26	SK.H.1	SkH	Text height	≧	1.00	O
	27	SK.MT. S.1	SkM	silkscreen to PAD distance	≧	0.20	O

Table 4.5.1-1 silkscreen design rule

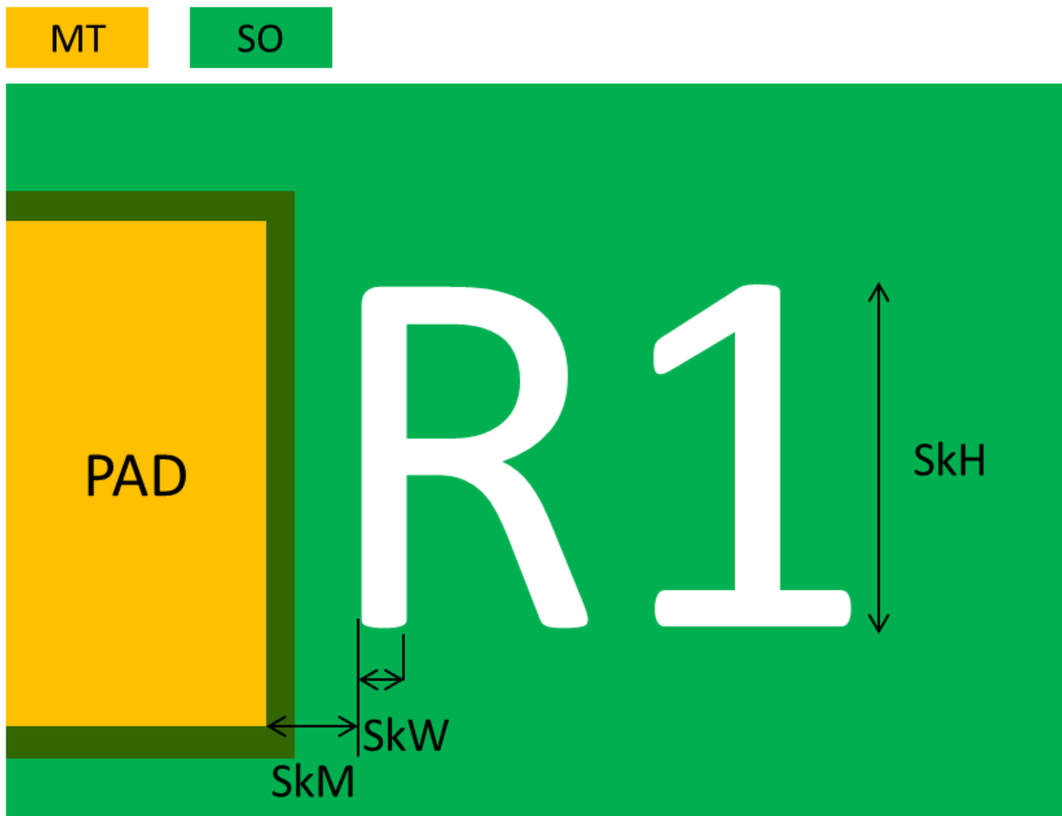


Fig. 4.5.1-1 silkscreen design rule

4.5.2 "PCB Identification Code" Marking

"PCB Identification Code" is text with a frame, marked at PCB board upper left corner, as the figure shown below.

Code format:

Process code_	**Year batch_**	**Self-naming**
2L_	**112A_**	**<u>4 digits of characters or numbers</u>**

Fig. 4.5.2-1 "PCB Identification Code" marking

4.6 Mechanical layer

Mechanical includes BO and ME2 layers:
BO layer: for PCB Board Outline (Board Outline)
ME layer: for ME Frame, PCB fabrication size and billing basis.
BO and ME frame distance: for Mechanical Milling cutter use.

4.6.1 PCB fabrication size, shape and billing

(1) Length / Width definition

PCB process code	PCB Fabrication contents	Unit Length(cm)	Unit width (cm)	max length (cm)	max width (cm)
PCB_2L	FR4 2-Layer Board	5	5	30	20
PCB_4L	FR4 4-layer board	5	5	30	20
PCB_2LH F16	RO 4003C HF 2-Layer Board	4.75	5.2	28.5	20.8
PCB_4L MX	RO 4003C - FR4 complex 4- layer board	4.75	5.2	28.5	20.8

Table 4.6.1-1 length / width definition

(2) Fabrication size: decided by ME frame,
(3) ME frame:

Length ≦ max length .ME frame

width ≦ max width

Shape: square, or rectangle

(4) Fabrication Shape: decided by BO frame, can be square, rectangle, polygons, or circles, etc.

(5) BO frame shape: Square, or rectangle, polygon, circle, etc.
See Figure below :(Red is ME frame, gray is BO frame.)

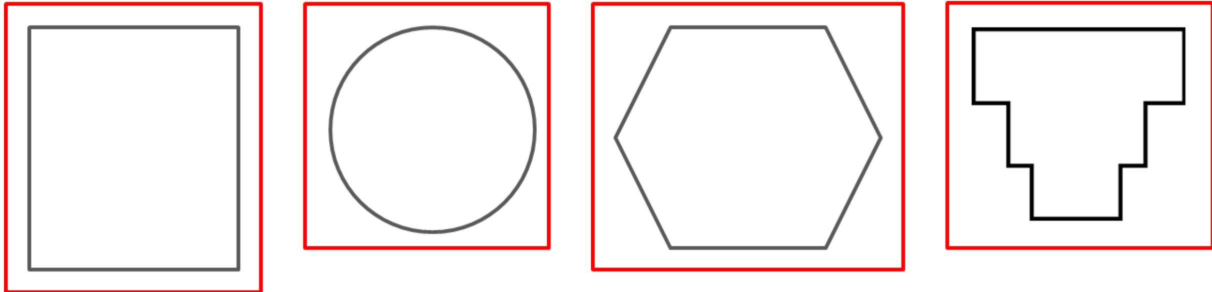


Fig. 4.6.1-1 PCB fabrication Shape

(4) Billing size: ME frame size,

(5) PCB Unit Area No.
Formula:

PCB Unit Area=(「ME frame length /Unit length 」 X (「ME frame width /Unit width 」)

Before multiplication, unconditional carry, the result is an integer.

EX: FR4 4-layer board application, ME frame length and width are 9cm and 6cm, then

Unit Area No. =(「9/5」 *(「6/5」) = unconditional carry = 2* 2 = 4

4.6.2 Board Outline BO frame and Position Hole NH design rule

(a) Board Outline: PCB Board Outline, i.e. BO frame, **MUST** draw on this layer.
(b) Other layer does not need BO frame.

(c) Position Holes: 4holes, Around BO frame corner, diameter ≧ 1mm NPTH:

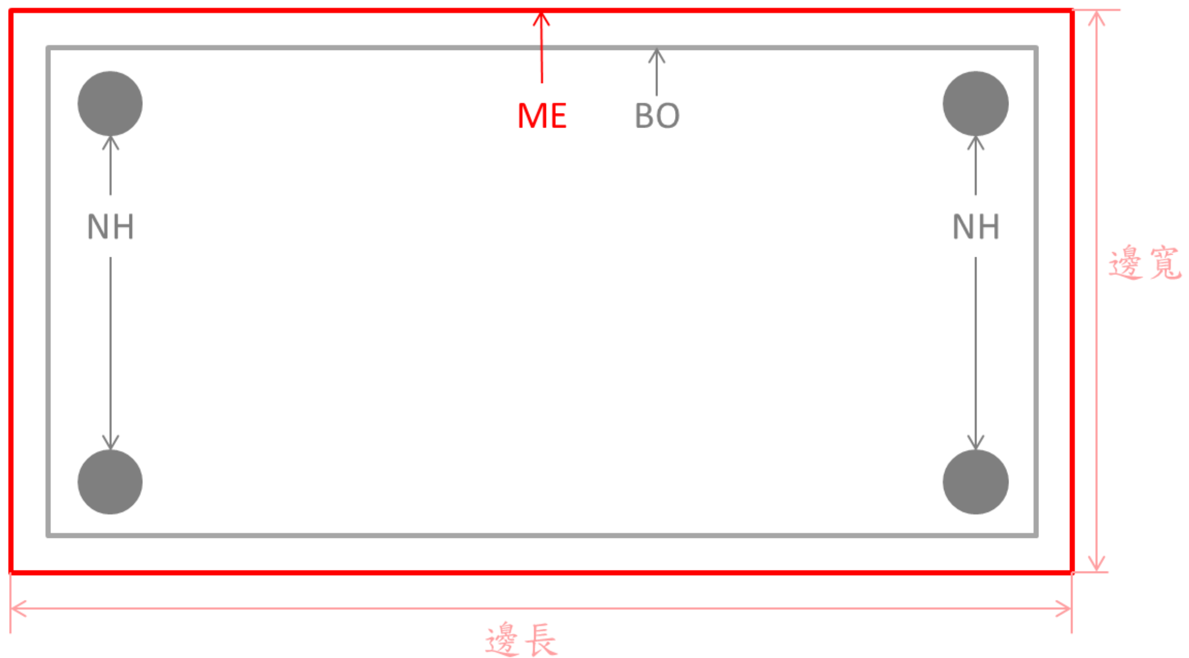


Fig. 4.6.2-1 Board Outline BO frame and Position Hole NH

Board Outline BO frame (gray line) and Position Hole NH (light gray circles) rule:

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
Mechanical layer BO	28	BO.W.1	BOW	Board Outline line width	=	0.10	M
	29	BO.H.1	NH	Position Hole diameter	≧	1.00	M
	30	BO.H.2	NH	Position Hole feature	=	NPTH	M

Table 4.6.2-1 Board Outline BO frame and Position Hole NH design rule

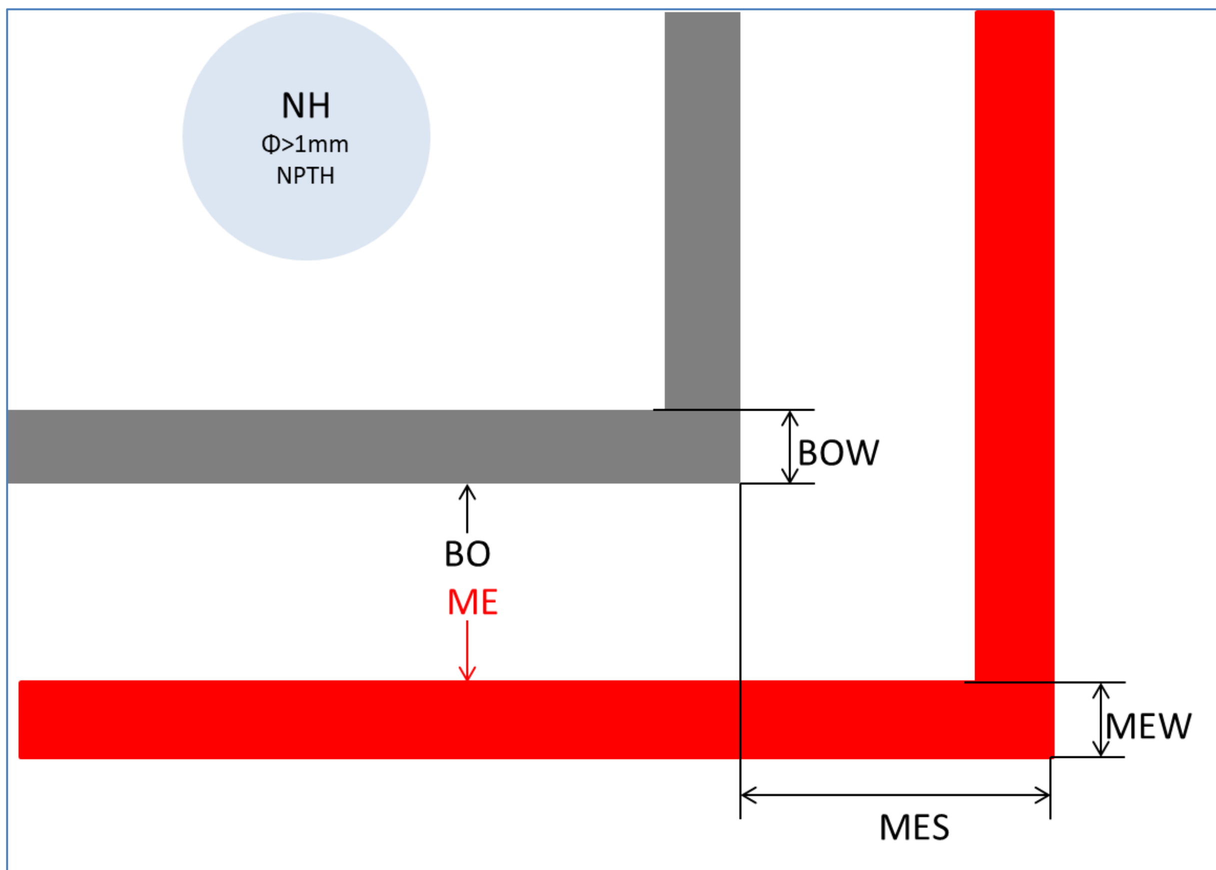


Fig. 4.6.2-2 Board Outline BO frame and Position Hole NH design rule

4.6.3 PCB cut out design rule

PCB cut out (Board Cut Out) is plotted on BO layer. The design rules:

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
Mechanical layer BO	31	CO.R.1	COR	PCB cut out edge arc diameter	≧	1.00	M
	32	CO.W.1	COW	PCB cut out width	≧	0.80	M
	33	CO.L.1	COL	PCB cut out length	≧	0.80	M
	34	CO.M.E.1	COM	PCB cut out and metal distance	≧	0.30	M
	35	CO.B.E.1	COB	PCB cut out and Board Outline distance	≧	1.60	M
	36	CO.T.1	COT	Text remark Cut Out	-	-	M

Table 4.6.3-1 PCB cut out design rule

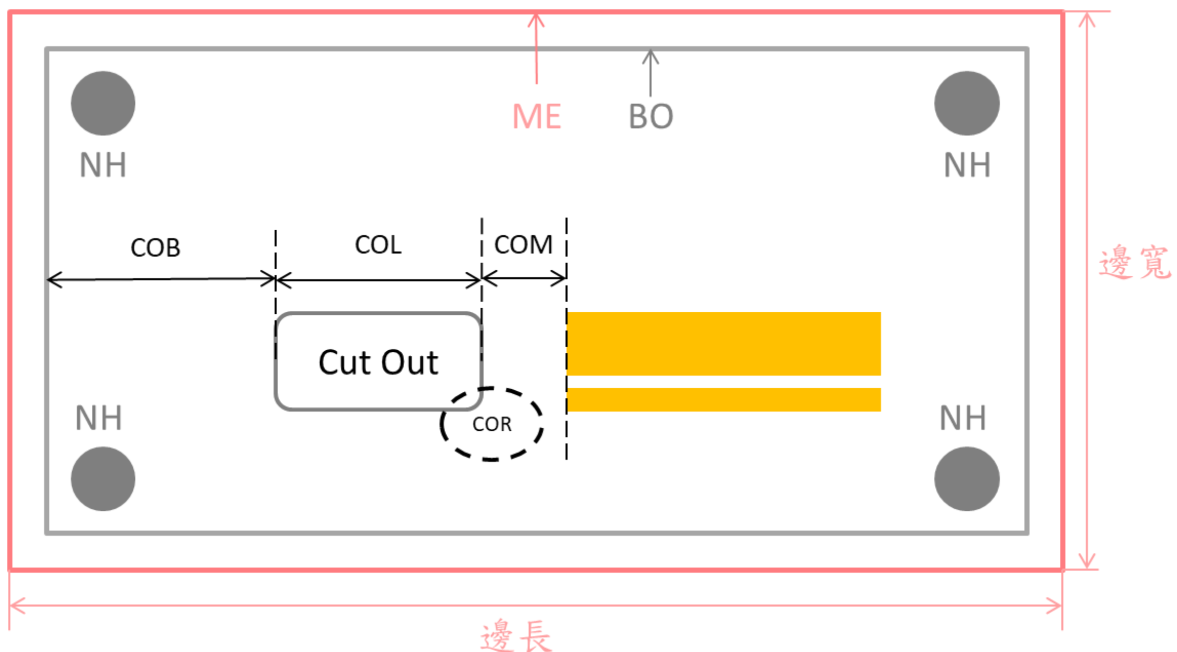


Fig. 4.6.3-1 PCB cut out design rule

4.6.4 ME Frame

4.6.4.1 ME frame design rule

Outside Board Outline (BO frame), draw an ME Frame ME frame. Its shape is square or rectangle. The distance to Board Outline = 1.5 mm. As the Figure shows. Red line is ME frame line.

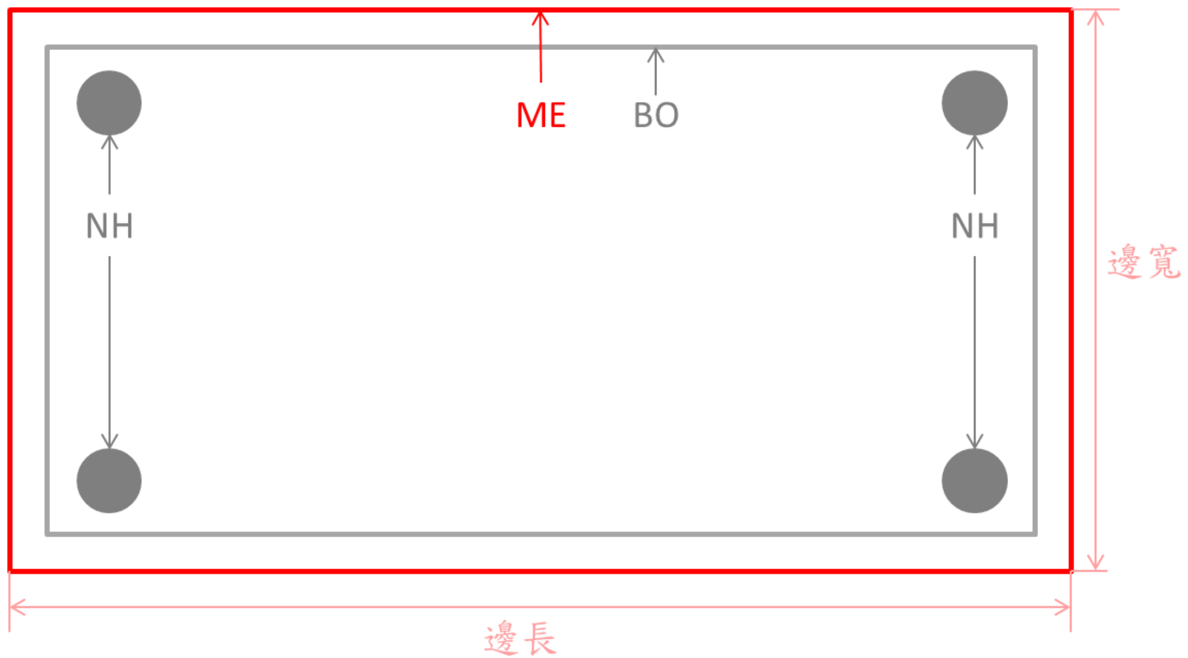


Fig. 4.6.4-1 PCB ME Frame ME and Board Outline BO frame

ME Frame (Red line) rule:

Item	No.	rule naming	code	Remarks	calculating signs	size (mm)	rule feature M / O
Mechanical layer ME	31	ME.W.1	MEW	ME Frame line width	=	0.10	M
	32	ME.S.1	MES	ME Frame to Board Outline distance	=	1.50	M

Table 4.6.4-1 ME Frame ME design rule

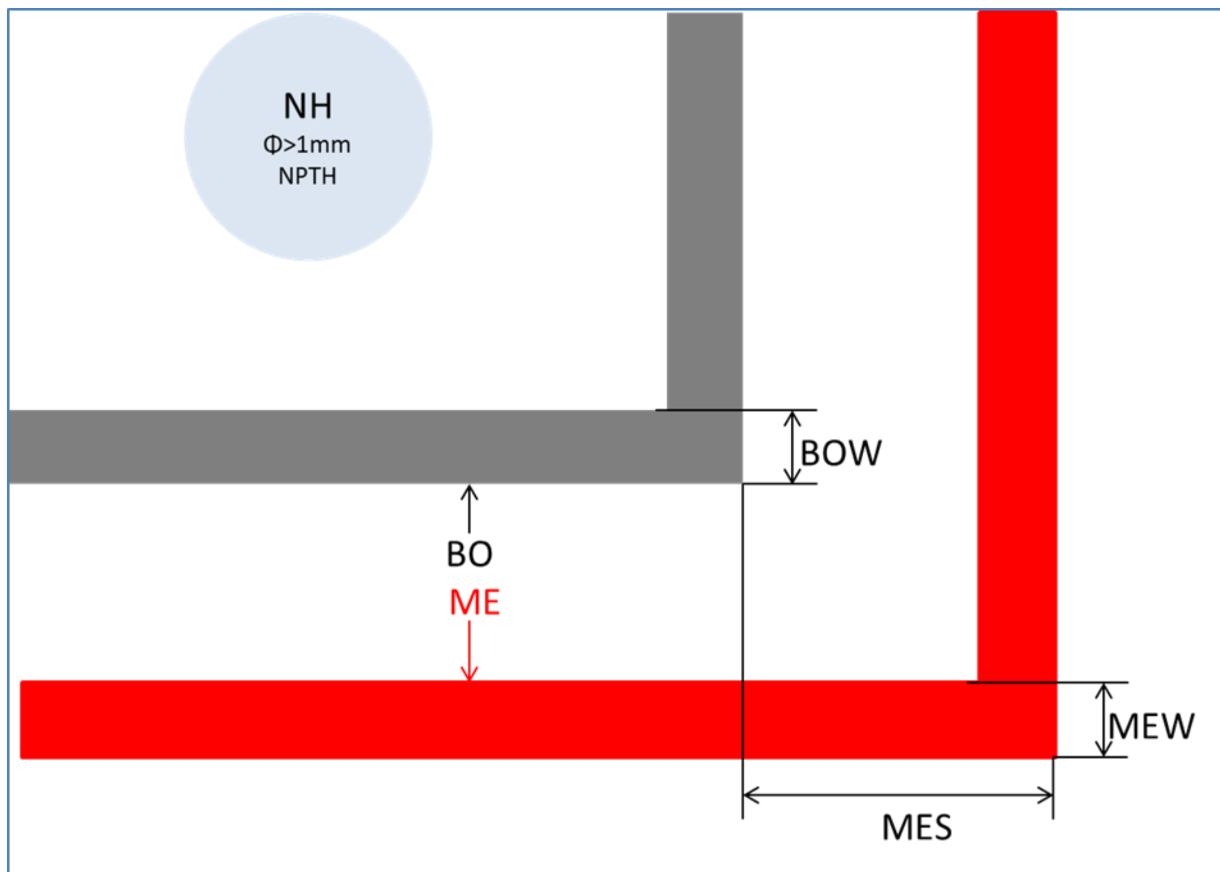


Fig. 4.6.4-2 ME Frame ME design rule

The above are TSRI PCB fabrication design rules.

5. Chinese and English noun contrast

English abbreviation	English Full Text	Chinese Full Text
BO	Board Outline	Board Outline
σ	Conductivity	電導率
DRC	Design Rule Check	設計規範驗證
DRM	Design Rule Manual	設計規範手冊
$ε_r$	Dielectric constant	介電系數
ENIG	Electroless Nickel Immersion Gold	化金，化鎳浸金
δ	Loss Tangent	損耗角正切
NPTH	Non- Plating Through Hole	不鍍銅貫孔
ME	Peripheral Outline	外圍邊框
PCB	Printed Circuited Board	印刷電路板
PP	Prepreg	膠片
PTH	Plating Through Hole	鍍銅貫孔
ρ	Resistivity	電阻率
	Solder Pad	焊墊
	Stacking	疊構
TPCA	Taiwan Printed Circuit Association	台灣電路板協會

6. References

6.1 PCB fabrication manufacturer

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6.6 PCB process video, Unimicron Germany company
https://www.youtube.com/watch?v=UAJ12W-VT2Q

6.7 PCB process video，科榮公司

http://www.youtube.com/watch?v=yZFfIKUd9pE