NARLabs 國家實驗研究院

國家奈米元件實驗室

NDL氮化鎵綠色功率元件服務平台
NDL GaN Power Device Service Platform

Guide

1. 本文件主要是用以協助在NDL使用氮化鎵功率元件服務平台的使用者。

2. 請使用者遵守文件中的指示進行製造。

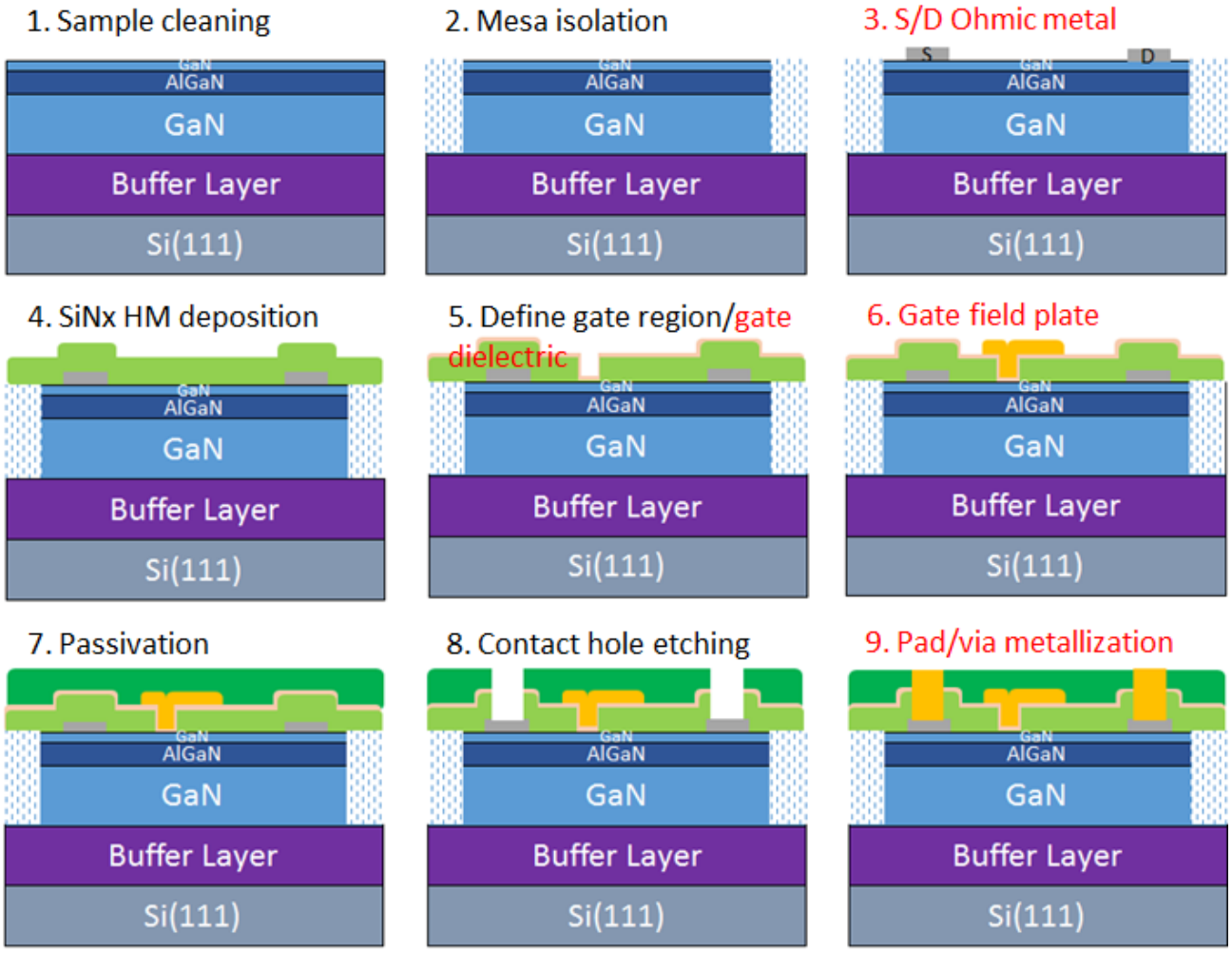
- 聯絡人: dylai@narlabs.org.tw (製程服務組 賴東彥)

Service Outline

- NDL提供標準空乏型(D-mode)功率元件製程，未來將提供增強型(E-mode)功率元件及射頻功率元件使用之T型閘極(T-gate)製程。
- 使用者需自備GaN-on-Si磊晶片，NDL不提供磊晶片或測試片。
- Baseline數據為元件製作於NDL標準磊晶片，元件特性會因不同磊晶片而有差異，請使用者下單前能理解。
- 基於標準範例元件製程，提供使用者改變元件佈局與金屬等材料進行驗證服務，需提供測試片供NDL製程測試。

- 聯絡人: dylai@narlabs.org.tw (製程服務組 賴東彥)

Baseline Process Flow



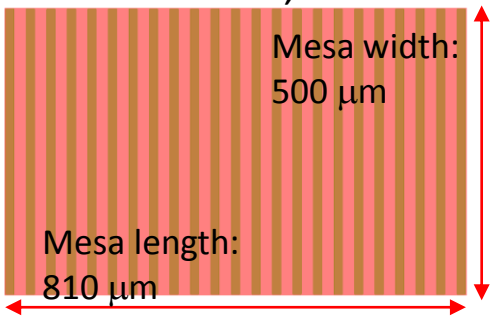
D-mode Schottky gate/MIS HEMT platform (6-inch/8-inch)

- Minimum resolution: L_G: > 1 μm
- Wafer bow < 40 μm, wafer thickness < 1000 μm

注意事項: 紅色字體為使用者可提供新材料，NDL提供元件驗證服務

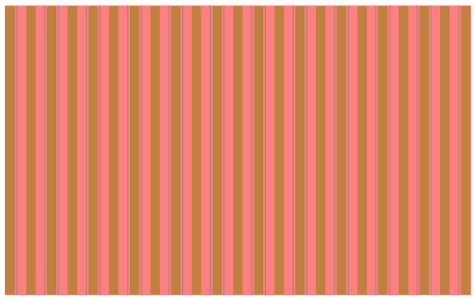
Baseline Layout

Mask 1, 2



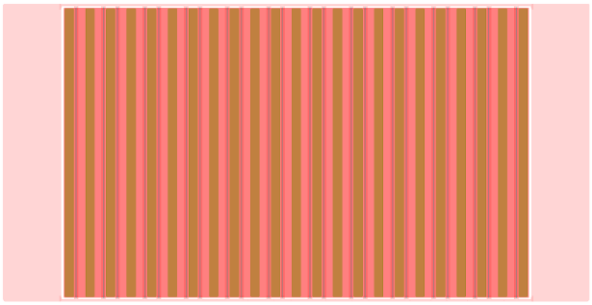
Mesa, S/D ohmic

Mask 3



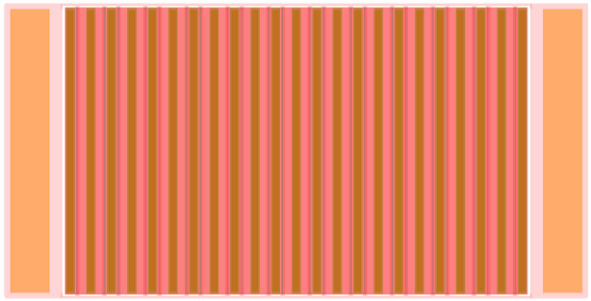
Define gate

Mask 4



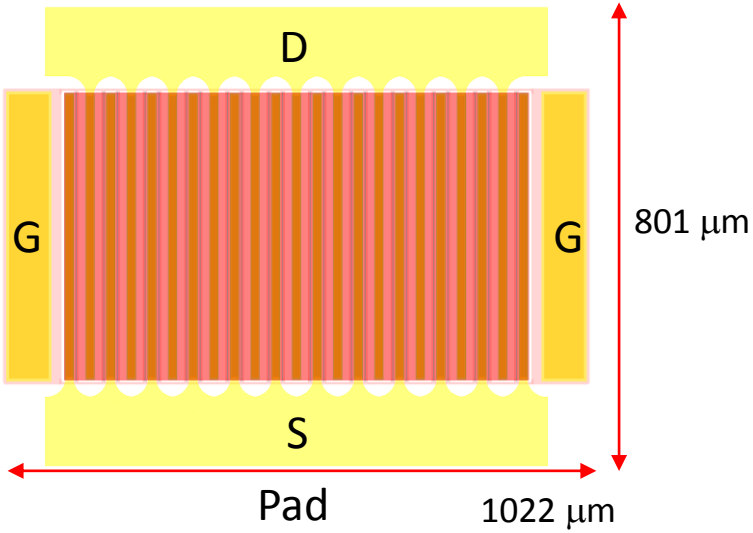
Gate field plate

Mask 5



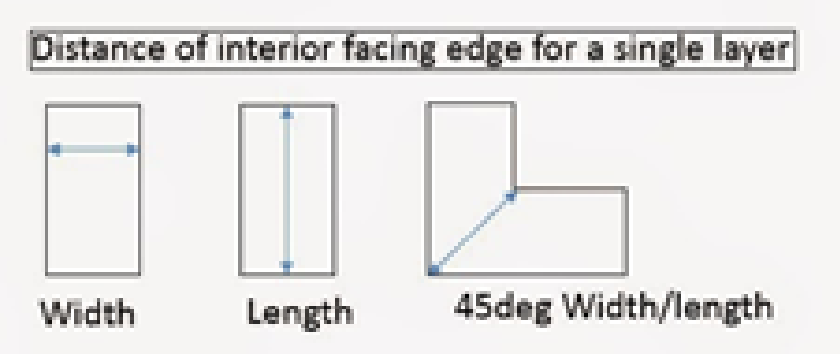
Contact hole

Mask 6

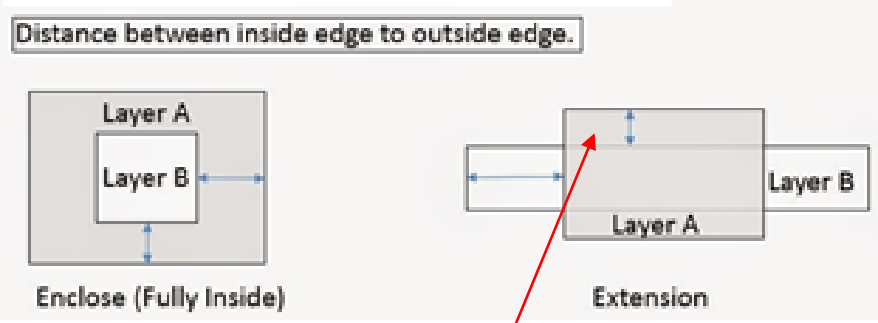


Design Rule of NDL Power Device

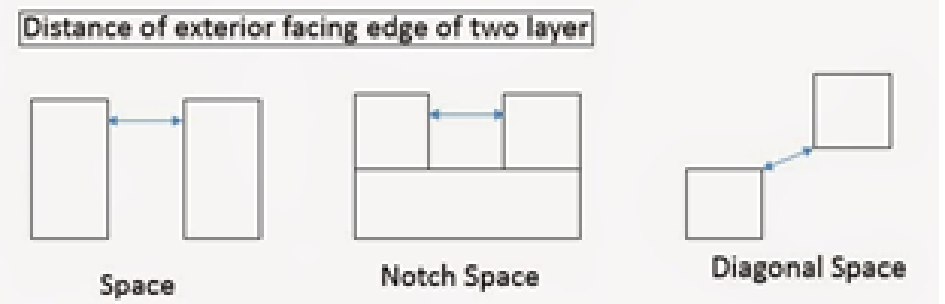
- Minimum pattern linewidth: 1 μm ± 0.5 μm



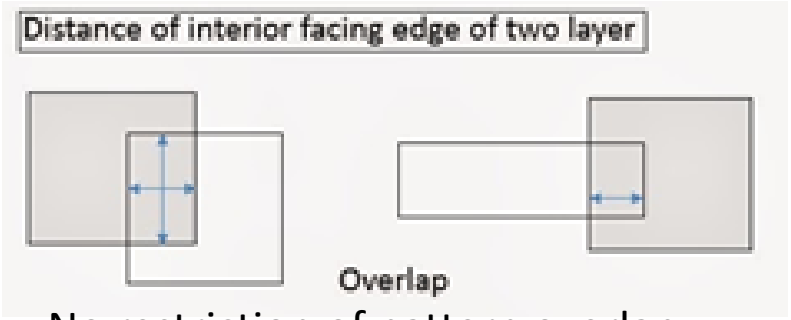
No restriction of curvature



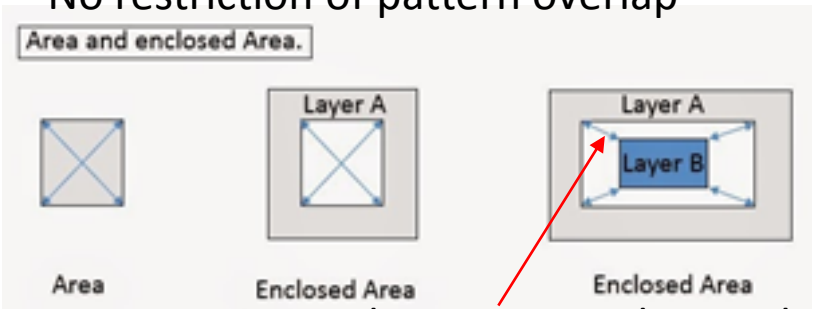
The extension between two layers should > 1 μm



Minimum spacing > 1 μm



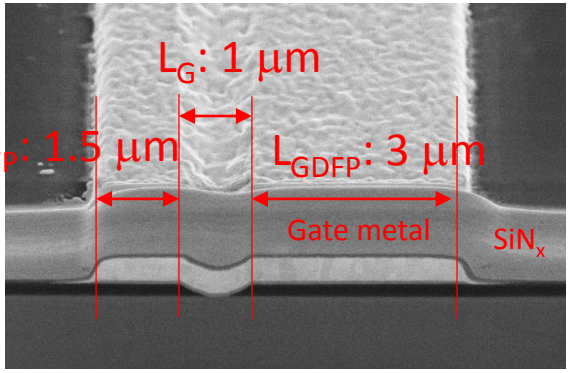
No restriction of pattern overlap



Minimum spacing between two layers should > 1 μm

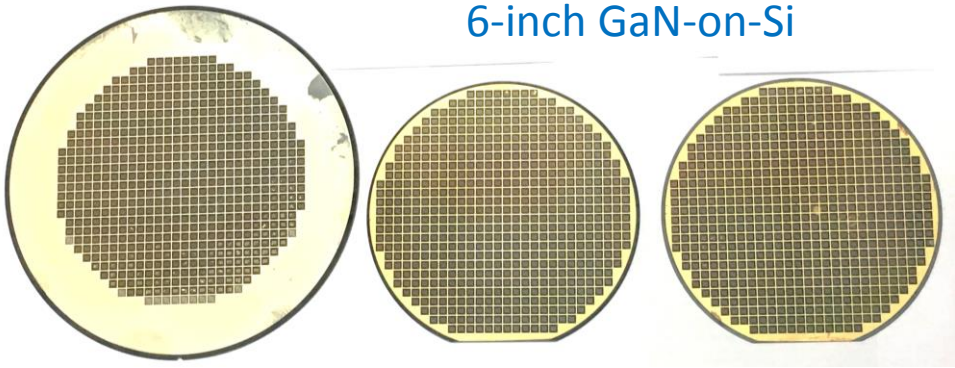
Baseline Device Performance

Gate FP SEM image



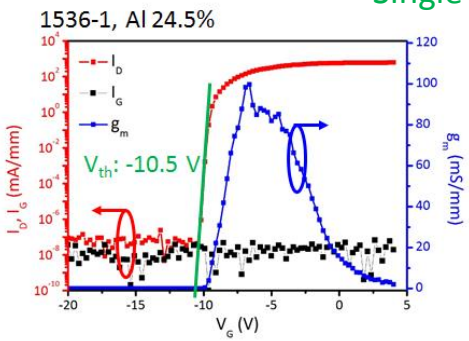
8-inch GaN-on-Si

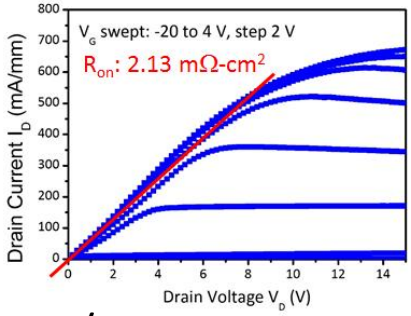
6-inch GaN-on-Si



D-mode GaN High Performance MIS-HEMT

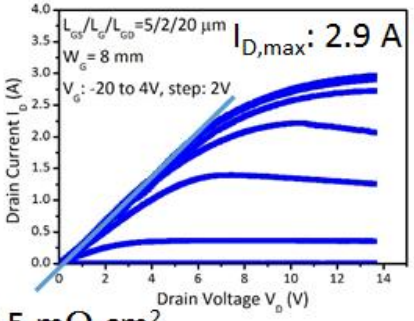
Single device

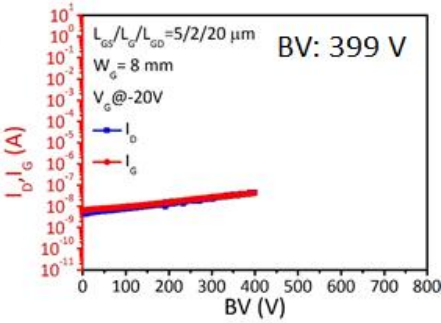




I_{on}/I_{off} > 10^8; Max g_m: > 90 mS/mm;
SS: < 100 mV/dec; R_{on}: < 15 mΩ-cm²

Interdigitated device (W_G: 8 mm)





R_{on}: 6.5 mΩ-cm²

Output current: 3 A, BV > 350 V

Baseline數據為元件製作於NDL標準磊晶片，元件特性會因不同磊晶片而有差異，請使用者下單前能理解。